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Research Result Report

ICRR Inter-University Research Program 2024

Research Subject: Development of a novel pulse generator system for the prototyping and testing of new trigger electronics for the ALPACA experiment
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Summary of Research Result：Gamma rays above 100 TeV open the possibility to study the acceleration mechanism and sources of CR in our galaxy. Gamma-ray astronomy at these energies is quite challenging, due to the dominant CR background. To this aim, the technique developed by the Tibet AS-gamma experiment, using a surface area array in conjunction with underground muon detector (MD) offers an powerful for background rejection. The ALPACA is a new air shower array is a new experiment between Bolivia, Japan and Mexico; using the same technique as Tibet AS-gamma. ALPACA is currently being installed at the Chacaltaya plateau and, when completed, it will be the first experiment to observe high energy gamma-rays in the southern hemisphere, pointing to the Galactic center. We are currently developing new front-end and trigger electronics for the experiment to enable its long term operation and also considering the future extension of the project to Mega ALPACA. Regarding the trigger electronics, fist we developed and tested a 32 channel system using and FPGA. In the fiscal year 2024 we advance in the development of a novel 128 output channel pattern generator. This novel device is capable of reproducing the timing and charge characteristics of the air shower experiment and will be useful to test the next prototype of the trigger electronics as well as the design of advance trigger techniques for ALPACA. The development of this system is done using a Zynq FPGA development board, which was bought using the budget from the Inter-University research program. A picture of this board is shown on figure one.

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The main characteristic of this board is that allows to implement complex logic systems and algorithms, because it combines a FPGA (programmable logic) with a CPU in the same integrated circuit.

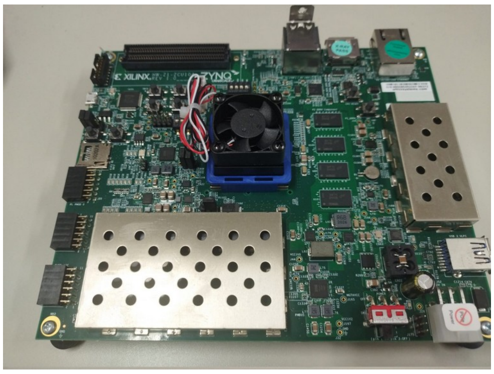

Figure 1. FPGA development board acquired for this project.

The architecture of this board allow us to build the system shown on the block diagram in Figure 2. In this case the CPU (PS in the block diagram) controls the reading of input parameters from a external memory (SD card) and stores them in RAM for fast access. The input parameters are the hit patterns and timing information from the MC simulation of ALPAQUITA.

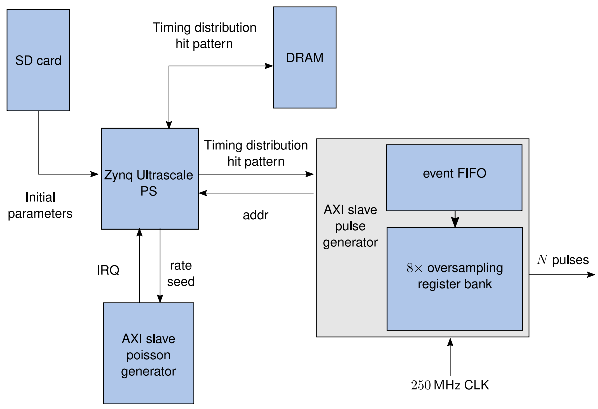

Figure 2. Block diagram of the pattern generator system.

The FPGA side is on responsible for generating the logical signal for each channel, taking into account the information provided by the processor. Using these two systems in combination, we are capable of generating patterns of 64 pulses at a maximum frequency 5 kHz (time between patterns), with a timing resolution between the pulses of the pattern of 0.5 ns. Due to the complexity learning to use the development board, we are still working on the evaluation of the performance of the system. A paper summarizing this research is under preparation.

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