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Electronics for the CREAM calorimeter and hodoscopes

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The electronics used for the CREAM calorimeter trigger and signal readout are based on 80 (32-channel) VA32-HDR2/TA32C chips digitized by 80 (12-bit) LTC1400 ADCs. The hodoscope electronics use 144 (16-channel) CR-1.4A chips digitized by 72 (16-bit) MAX1133 ADCs. The basic characteristics, such as noise level, dynamic range, linearity, and gain of both systems were measured in the laboratory. The results confirm that the design goals of the CREAM experiment could be achieved.

1. Introduction

The CREAM experiment [1] is intended to be flown at the top of the atmosphere under NASA research balloons to directly measure cosmic-ray nuclei and reconstruct their individual spectra. CREAM is planned to be the first payload of the Ultra Long Duration Balloon being developed by NASA. This balloon is expected to fly between the 30th South parallel and the South Pole. As such the payload will need to operate on stored power for up to 12 hours at a time. During daylight, solar arrays will power the instrument and support systems, while recharging the bank of batteries in the power system. Due to the limited weight available for the payload, and specifically for the power system, the instrument power needed to be kept as low as possible. This requirement directed the readout design of the calorimeter and hodoscopes to Application Specific Integrated Circuits (ASICs) with multiple channels per ASIC. The design goals included low noise levels to allow sufficient S/N ratio for both detector systems, and sufficient linear dynamic range to cover the expected signal ranges.

2. Readout electronics design

The calorimeter front end electronics are housed in four HPD boxes (Fig. 1), each with 10 HPDs socketed in a Front board at the top of the box. Each HPD reads out 55 channels, of which 25 are low-range, 25 mid-range, and 5 high-range, based on the calorimeter optical division scheme [2]. At the bottom of the box a pair of Motherboards holds the connectors to the data sparsification system, the trigger system, the command system, the calibration system, and the power system. The Motherboards also provide the HPDs with bias voltage. A set of 10 ASIC boards connects the Front board and the two Motherboards. On the outside of the box, a pair of High Voltage Power Supplies (HVPSs) provides filtered high voltage, up to 12 kV (adjustable) at up to 1 μA each. The HV connections pass through a bleeder circuit to allow a relatively fast bleed-down through 15 GOhm resistance to ground once the HVPSs are turned off (~30 seconds). The bleeder circuits also include monitor resistors to verify HV levels through the housekeeping system, and current limiting resistors to protect against shorts. The HV system is fully potted in EN-4/EN-11 sealant, with semi-resistive coating painted on external surfaces to bleed down surface charging. Where the HV wires come out of the potting, a staking compound continues the seal to prevent HV discharging at flight altitude where the ambient pressure is typically a few millibar. On the outside of the HPD boxes a pair of LED light sources is mounted and connected via jacketed clear plastic fiber bundles to 4 pixels on each HPD, to provide for alignment verification pre-flight and in-flight aliveness test for the HPD. The LED sources are pulsed by the calorimeter calibration board. Each calorimeter HPD is read out by a pair of VA32-

HDR2/TA32C ASICs, for a total of 80 such ASICs. These ASICs provide a linear dynamic range of about 1:1800, and require about 3.5 milliwatts per channel. Each pair of VA/TAs is socketed in an ASIC board, allowing convenient replacement in case an ASIC is damaged before flight. The ASIC board also holds 12-bit LTC1400 ADCs, protection diodes, line drivers, etc. Each VA/TA ASIC has 32 signal input channels, a 32-channel serial output and one trigger output channel. The VA receives the input signals, and passes them through a Gaussian shaping circuit, and into a hold-circuit after an adjustable peak-hold delay. The TA passes the input signals received from the input stage of the VA through a fast semi-Gaussian shaper, and compares the levels to an adjustable preset threshold. If any of the 32 shaped signals exceeds the threshold, the TA sends out a trigger signal, and the ASIC board sends the stored charge values to the ADC. The digitized signals are sent through the Motherboard to a sparsification system that discards those signals that are below sparsification thresholds (adjustable on a channel by channel basis). This reduces the bandwidth required for data telemetry to the ground to manageable levels.

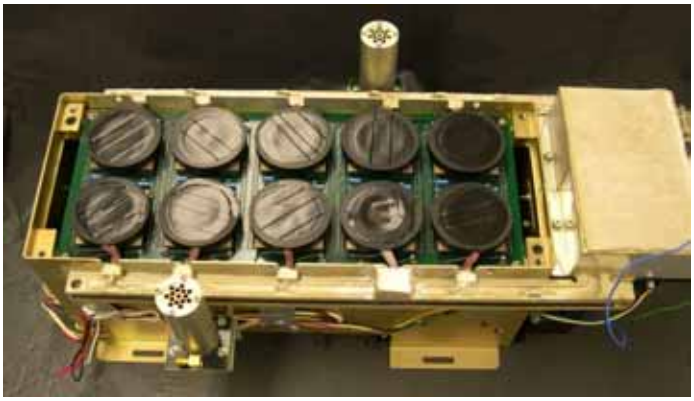

Figure 1. Calorimeter HPD box with EN-4/EN-11 HV potting

In the hodoscope readout system, the 36 HPDs are each socketed in a separate Front board, with a stack of three more small form factor boards: ASIC board, Shield board, and Interface board to complete a single HPD box. The hodoscope HPD boxes are designed to allow the Front board to be mounted directly to a front panel that can be maneuvered to align the HPD to a hodoscope fiber cookie. Once this is achieved, the front panel is not moved unless the HPD needs to be replaced. This maintains the alignment and calibration to the greatest extent possible. The stack of three boards is mounted using four long screws that pass through the boards and spacers, attaching to stand-offs mounted through the Front board and into the front panel. This electronic stack is then covered with a shielding box. Each HPD has a special 15 kV cable connecting it to a Motherboard mounted in a separate Motherboard box on the main pallet of the payload. Each Motherboard has one HVPS powering three HPDs, and reads out those same HPDs' ASIC boards through their Interface boards (Fig. 2). In this system too, a bleeder circuit with current limiting resistors is potted in EN-4/EN-11 sealant. In the hodoscopes, the light yield for the smallest signals is insufficient for

Figure 2. Hodoscope readout setup with Motherboard box, HVPS and 3 HPD boxes

optical splitting as was done in the calorimeter, thus the linear dynamic range required in this system is greater than that provided by the VA/TA system. The ASIC chosen for this system was the Amplex-type CR-1.4A. This 16-channel ASIC was also flown as part of the Silicon Charge Detector (SCD) readout in the ATIC payload [3]. It provides a linear dynamic range of ~1:8000, sufficient for the hodoscope readout. The power requirement is 5.6 milliwatts per channel in the ASIC.

3. Test results

The characteristics of the two ASIC types, VA/TA and CR, were tested in the lab using the relevant flight front end electronic boards. The pulse shape of each chip was plotted (Fig. 3) by measuring the gain, averaged over the 32 VA/TA channels or 16 CR channels, for a variety of readout delay times. The average peak delay time was ~1.5 μs for the VA/TA, and 1.8 μs for the CR. Figure 4 (a) shows a gain distribution of all 2560 channels of the calorimeter VA/TA chips. The mean value of 0.98 (ADC/DAC) corresponds to

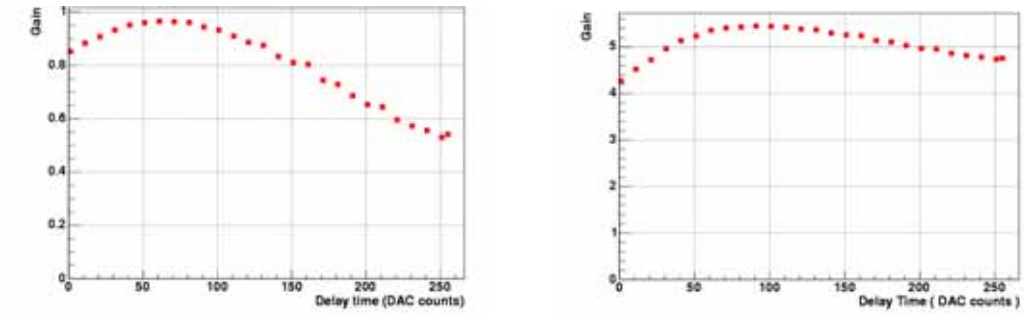

Figure 3. Measured pulse shape averaged over all channels for (a) calorimeter VA/TA chip, and (b) hodoscope CR chip.

about 0.88 mV/fC as measured in the lab. Figure 4 (b) shows a distribution of pedestal RMS noise for all 2560 VA/TA channels. The mean value of 1.085 ADC counts is ~1.23 fC (~7700 e) or ~54% higher than the nominal VA/TA spec of ~5000 e. The noise of the hodoscope's CR chip is ~7 counts in a 16-bit ADC, corresponding to 0.93 fC (~5800 e). The gain of the CR chip is typically ~0.93 mV/fC. Figure 5 shows the

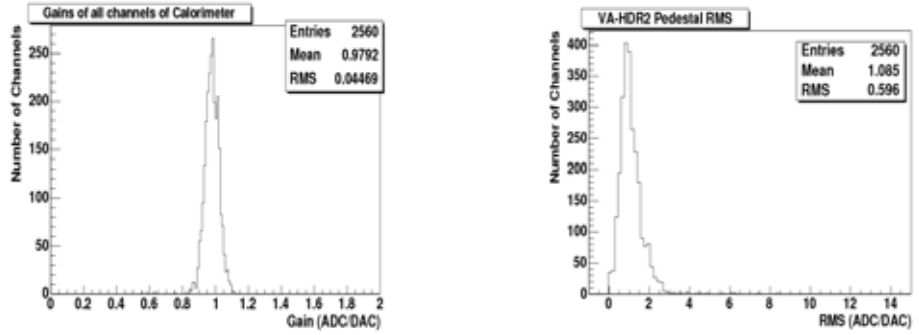

Figure 4. Measured (a) gains and (b) pedestal RMS of all 2560 calorimeter VA/TA channels.

linear dynamic ranges for both chips averaged over all 32 or 16 channels. The VA/TA has a linear dynamic range of 1:1000 (1100 ADC counts above pedestal, or ~1 pC with ~1.1 ADC counts noise), and the CR has a linear dynamic range of 1:4000 (30000 ADC counts above pedestal, or ~4 pC with ~7 ADC counts noise). Finally, the trigger part of the VA/TA was tested and found to have a gain of ~2.85 DAC-counts-at-threshold/ADC-counts, as seen in Fig. 6. The fitted noise level of the TA circuit is ~13 DAC counts (~ 4.5 ADC counts). Reducing trigger noise at a 5σ level requires a minimal threshold level of ~22.5 ADC counts.

4. Conclusions

Custom electronics were developed for the CREAM calorimeter and hodoscope readout systems. Design requirements included low noise, large dynamic range, low power, and high channel count. The 32-channel IDEAS VA32-HDR2/TA32C ASIC was chosen to provide readout and triggering for the calorimeter, while

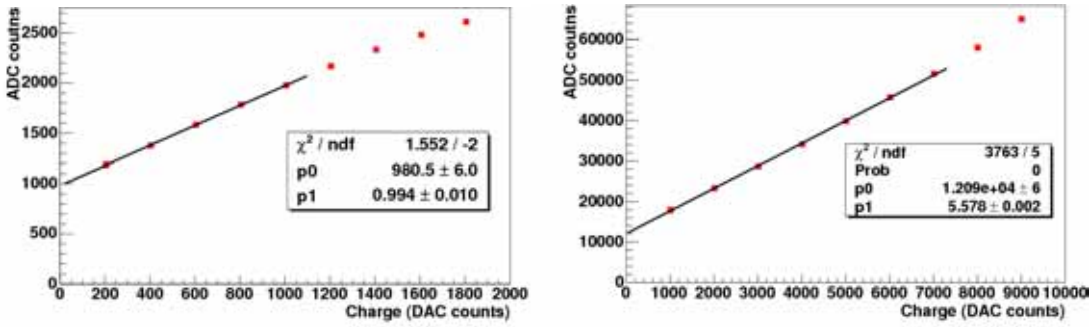

Figure 5. (a) Charge calibration run averaged over 32 channels of a VA chip, linear up to ~2100 ADC counts (~1 pC); (b) charge calibration run averaged over 16 channels of a CR chip, linear up to ~40000 ADC counts (~4 pC).

the 16-channel Amplex-based CR-1.4A ASIC was chosen for the hodoscopes, where optical signal division was impractical and its greater dynamic range was required. Lab measurements of these two chips, mounted in the flight electronics proved the noise level was sufficiently low, the linear dynamic range sufficiently high, and power dissipation sufficiently low to meet the tight constraints of a balloon-borne instrument such as CREAM. The high channel multiplicity of these chips was a good match for the 2200 calorimeter signal channels and 2035 hodoscope signal channels, allowing the front end electronics packaging to be sufficiently compact to fit in the space available.

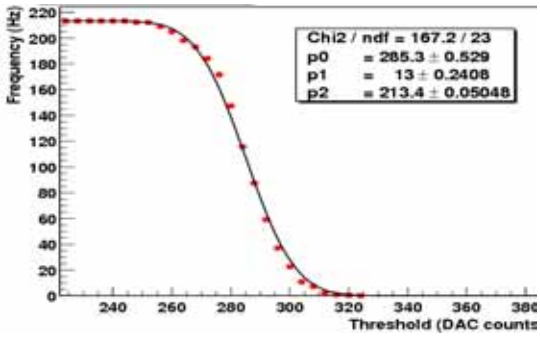

Figure 6. Trigger gain measurement for a typical channel of a VA/TA chip with a charge input of 100 DAC counts (~0.1 pC), showing a gain of about 2.85 DAC/ADC.

5. Acknowledgements

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References

[1] E. S. Seo et al., *Advances in Space Research*, **33**/10, 1777 (2004).
[2] O. Ganel et al., Proc. 10th Int. Conf. Calorimetry in Part. Phys., Pasadena, 133-138 (2002).
[3] J.H. Adams Jr. et al., OG 4.1.18, Proc. Of the 26th ICRC, Salt Lake City (1999)