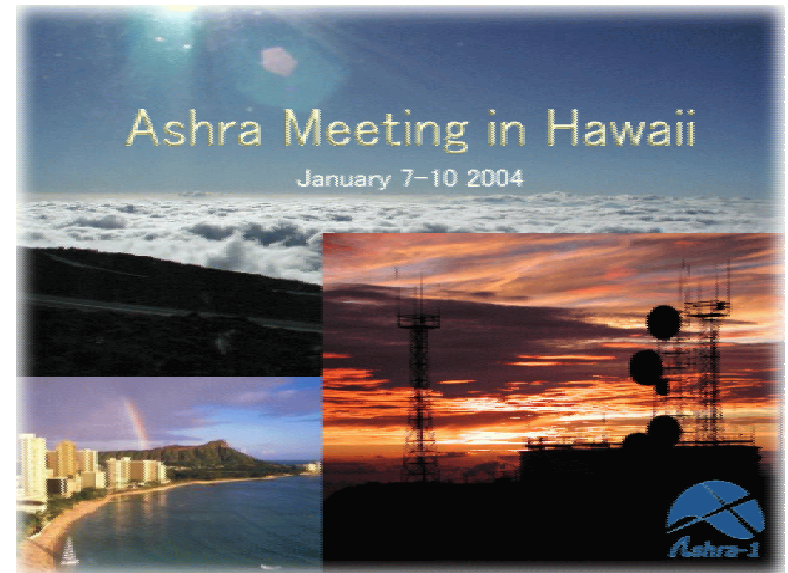




Ashra CMOS Fine Image Sensor

*Jan. 8, 2004, @U. of Hawaii
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- Introduction
- Sensor Architecture
- Pixel Structure
- Signal Simulation
- Schedule



Introduction (1)

CMOS sensor technology is rapidly progressing. It has many advantages compared with CCD technology;

- It is possible to integrate with logics (High Performance).
- Commercial process is usable (Low Cost).
- It works in low voltage (Low Power).
- Higher S/N becomes achievable with circuit technologies (close to CCD).
- High-speed readout is possible with pipeline and/or parallel techniques.

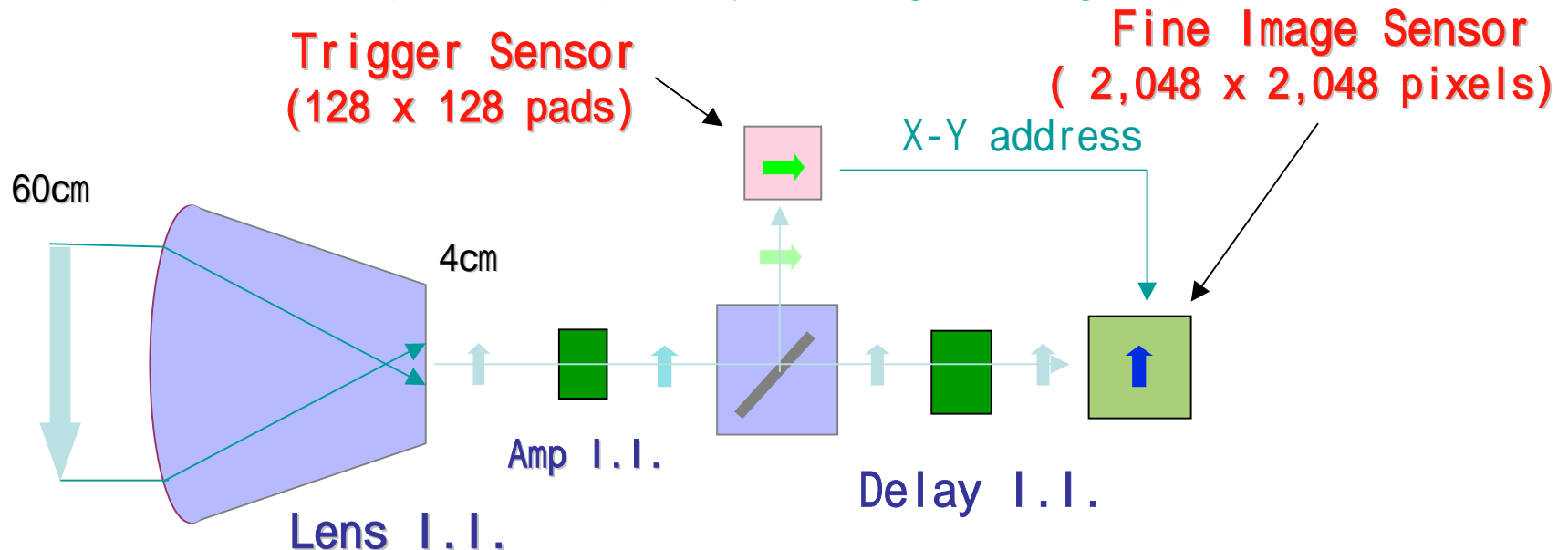
However existing CMOS sensor has;

- A global shutter -> to cover large FOV, shutters for small regions are necessary to avoid unwanted light background.
- < 10 frames/sec -> higher readout rate (~1,000 event/sec) is required to reduce trigger threshold. We should read out only interesting parts of sensor.

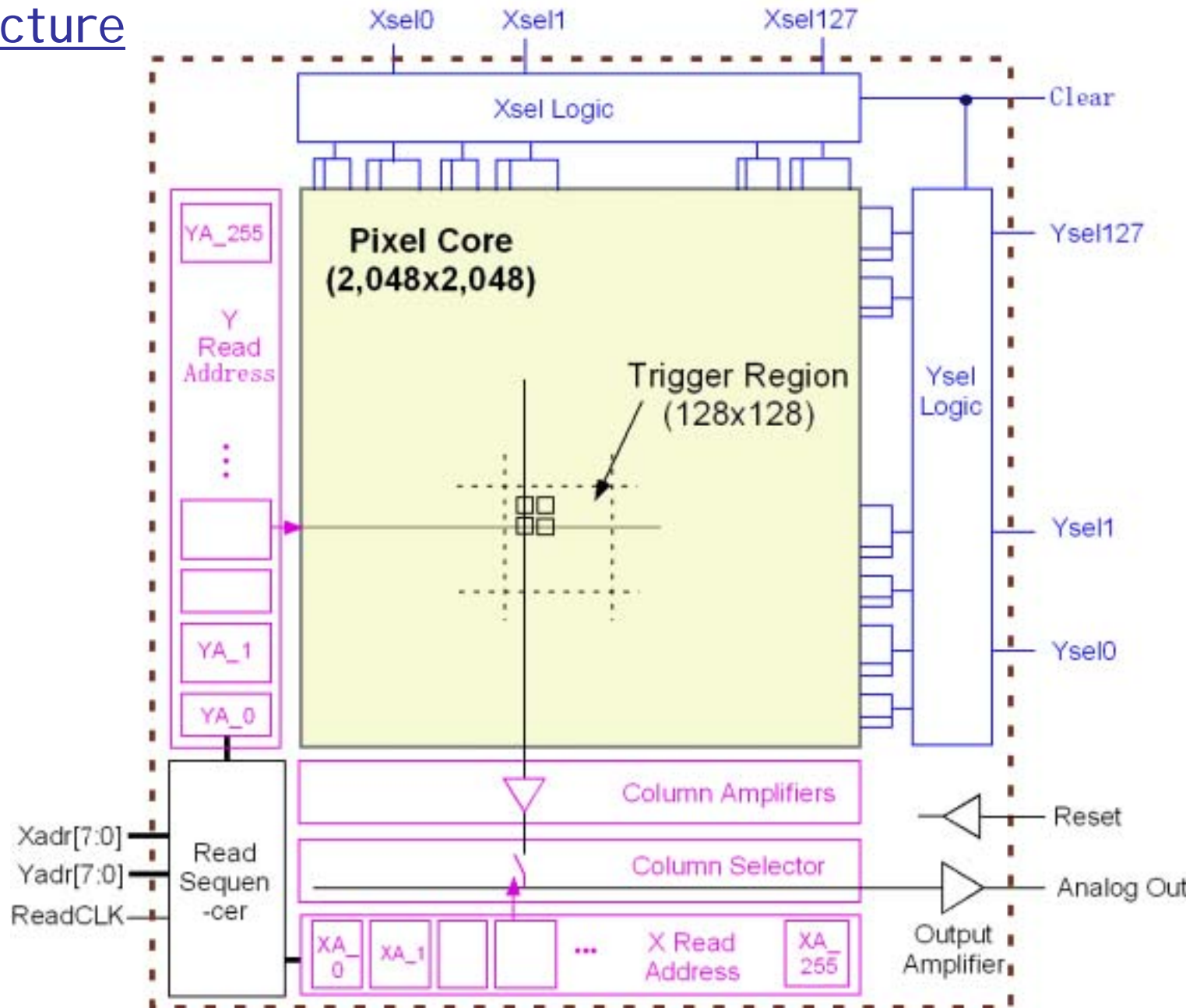
➔ Develop New CMOS sensor !

Introduction (2)

- To achieve 1 arcmin resolution, 3,000x3,000 pixels are required, but we select **2,048x2,048 pixels** (1.5 arcmin) fine image sensor (AFS-1) as a realistic solution at present stage.
- 2-D selectable (128 x 128 regions) exposure to reduce background noise.
- 2-D selectable (128 x 128 regions) readout to reduce deadtime.
- Overlapping exposure for triggered region should be possible.
- Use advanced CMOS process (0.25 μm) to get large aperture.

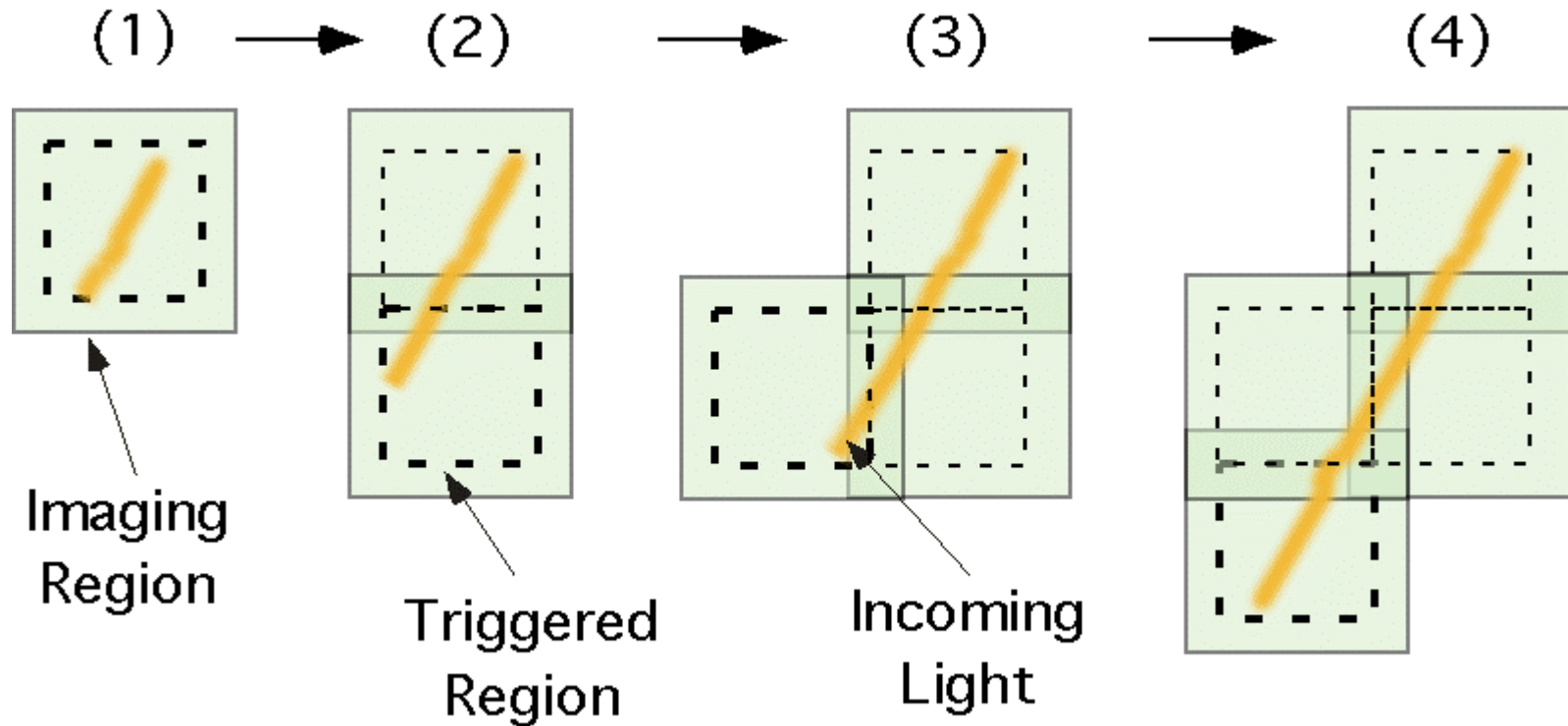


AFS-1 Structure



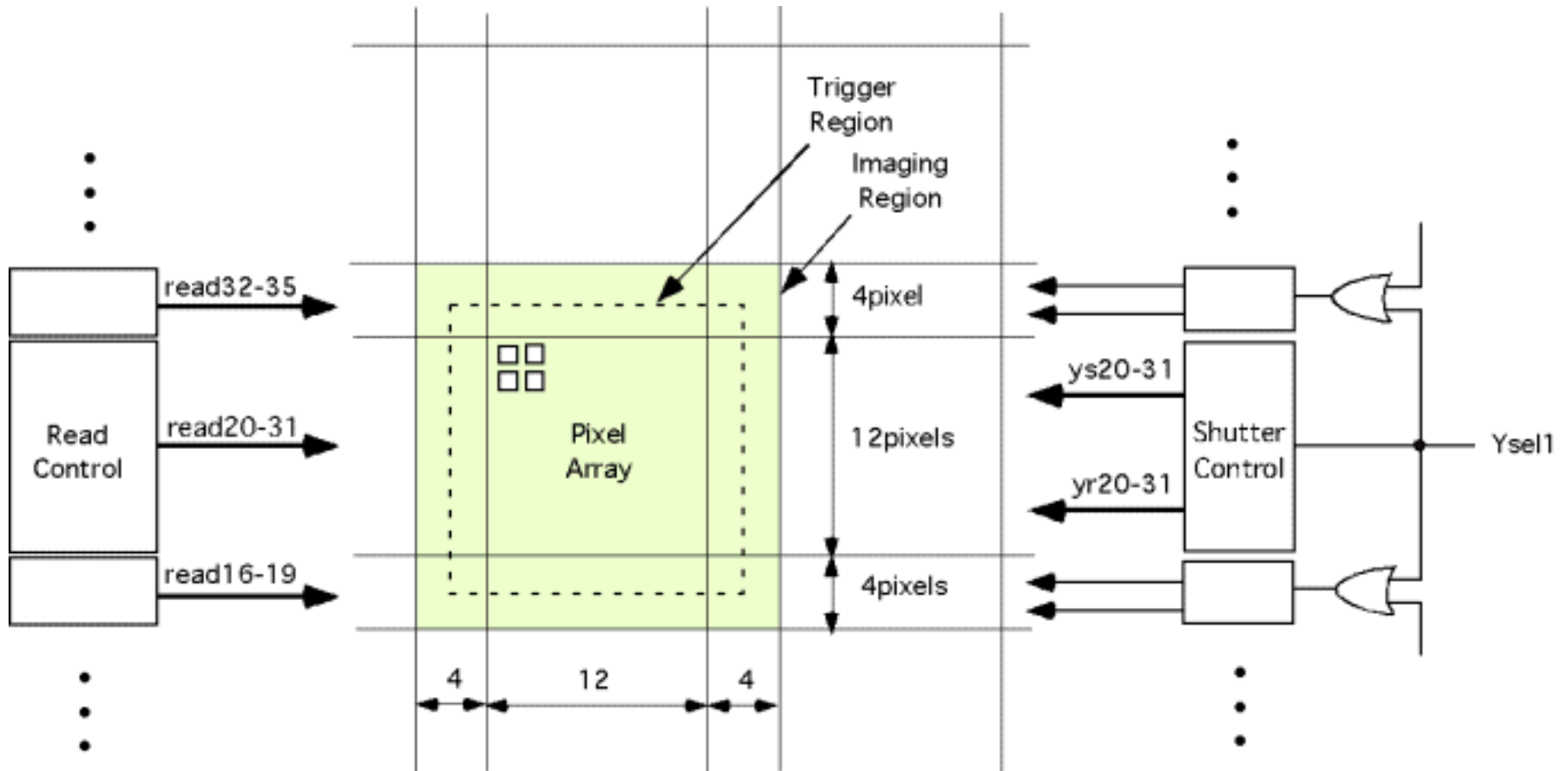
Overlapping Imaging

Imaging region should be larger than the triggered region to compensate misalignment.



Region Control Logics

- A trigger region is composed of 16x16 pixels.
- Imaging region has 20x20 pixels, thus 4 pixels overlap with adjacent region.
- Readout is done for each sub regions.

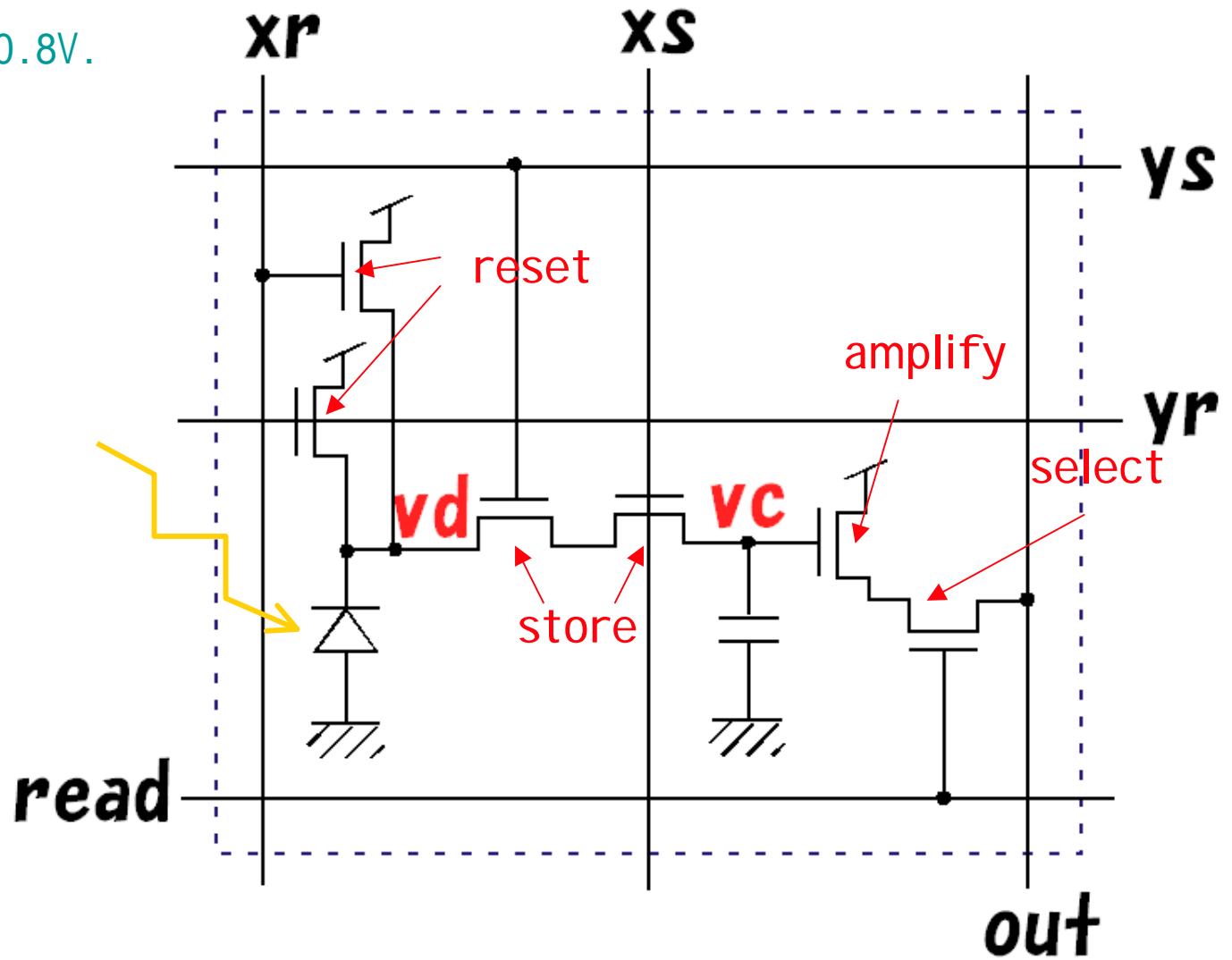


(Same logics in X-direction)

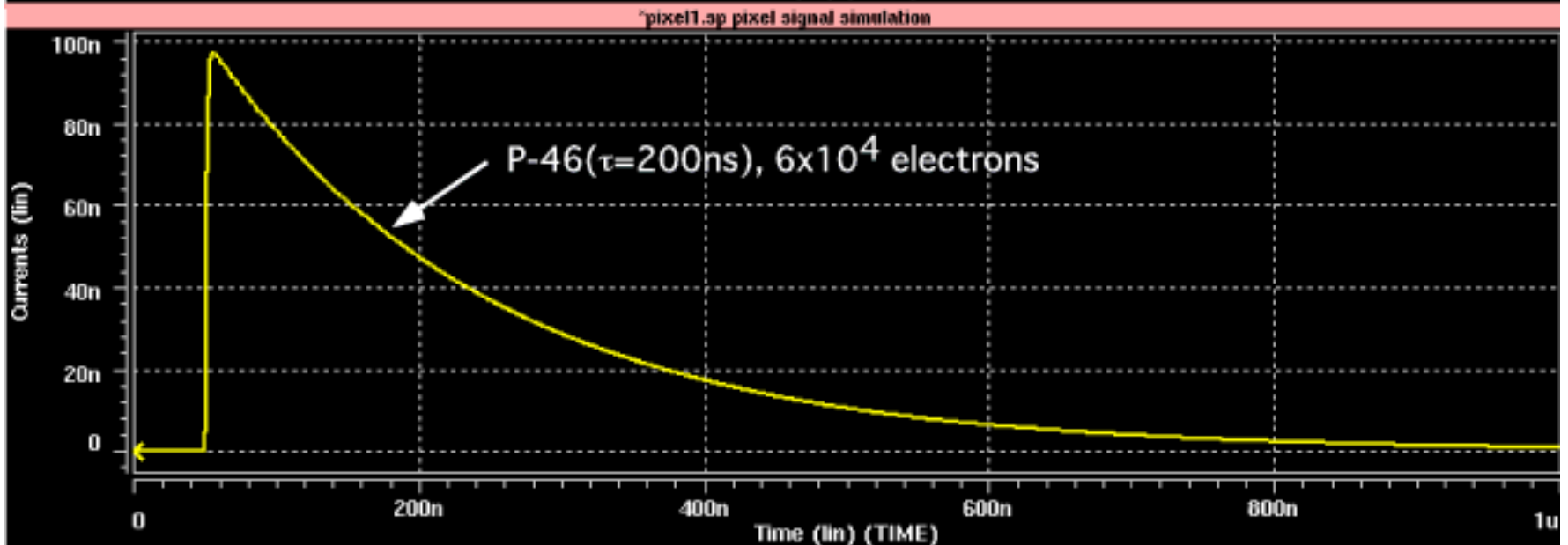
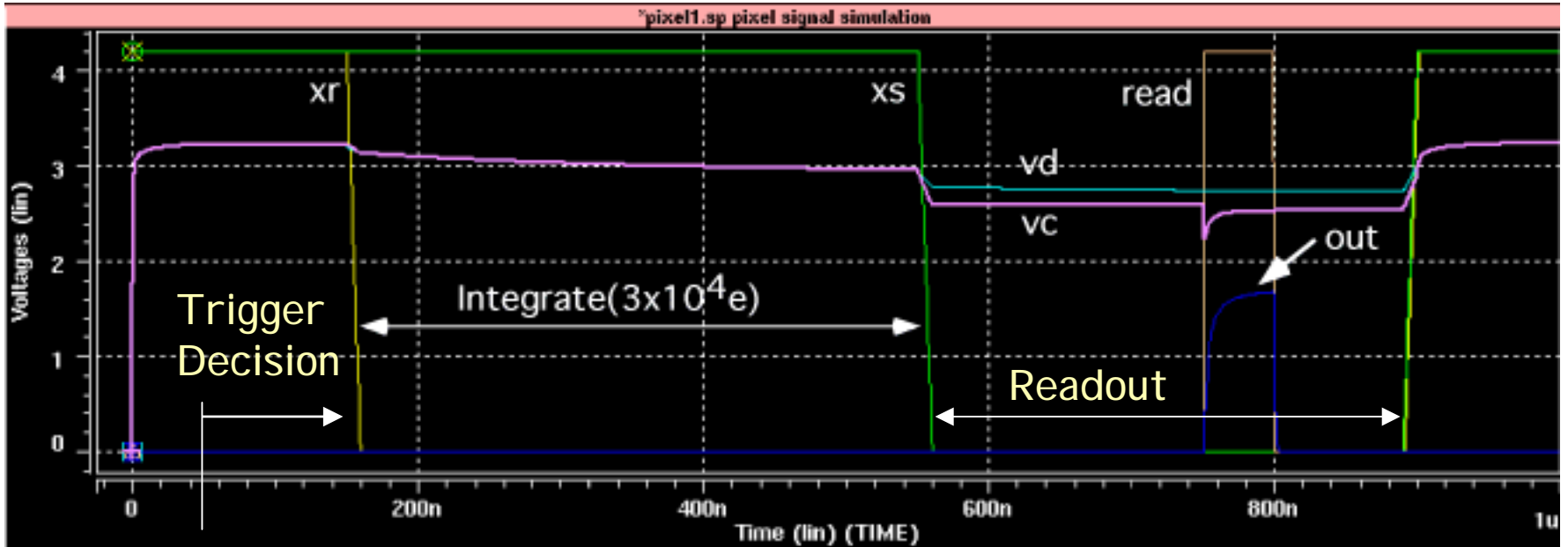
An example of 2-D CMOS Active Pixel

Pixel use only NMOS Tr.

$V_{control} > V_{dd} + 0.8V$.

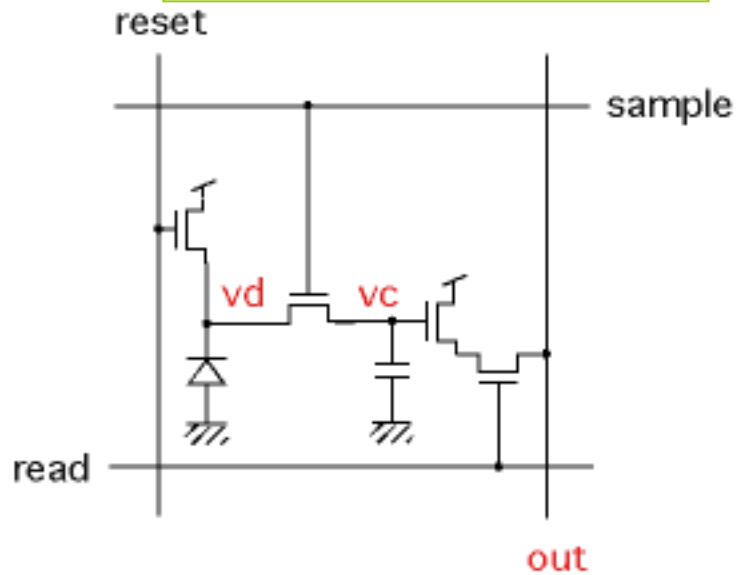


A Toy simulation of Light Exposure with a Delay I.I.



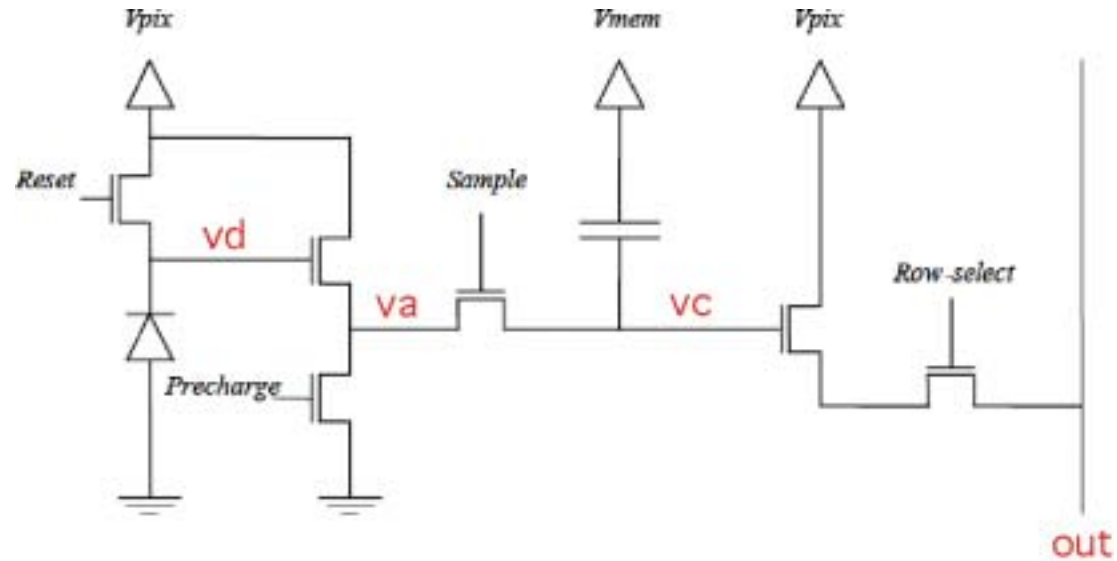
Pixel Structure (1-D)

4-Transistors (IBIS5)



- Simple
- Small pixel area
- Capacitance of vd node must be small to have high gain ($V=Q/C$)
- S/N is relatively low

6-Transistors (LUPA-4000)

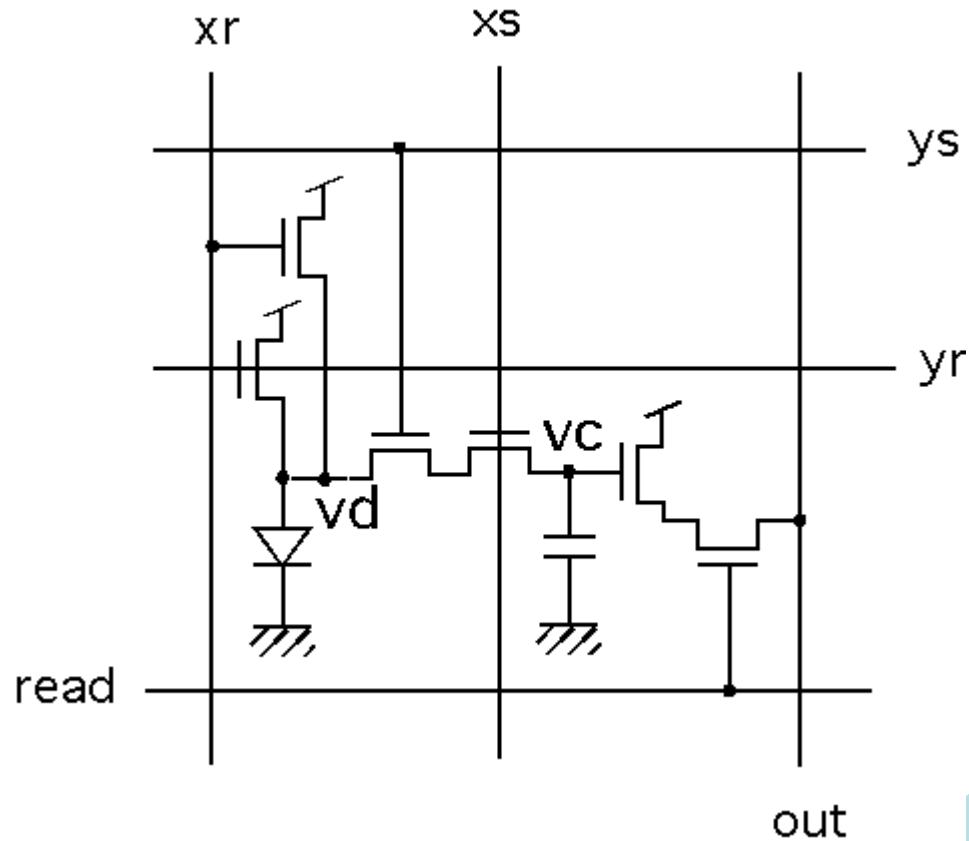


- High Voltage/Charge gain
- S/N is relatively high
- Pipeline operation is possible
- Control is rather complicated.
- 2 additional transistors (Larger pixel area)

Naive Extension of 4T cell to 2-D

No. of Transistors : 4 -> 6 Tr

No. of Control Line : 3 -> 5 lines.

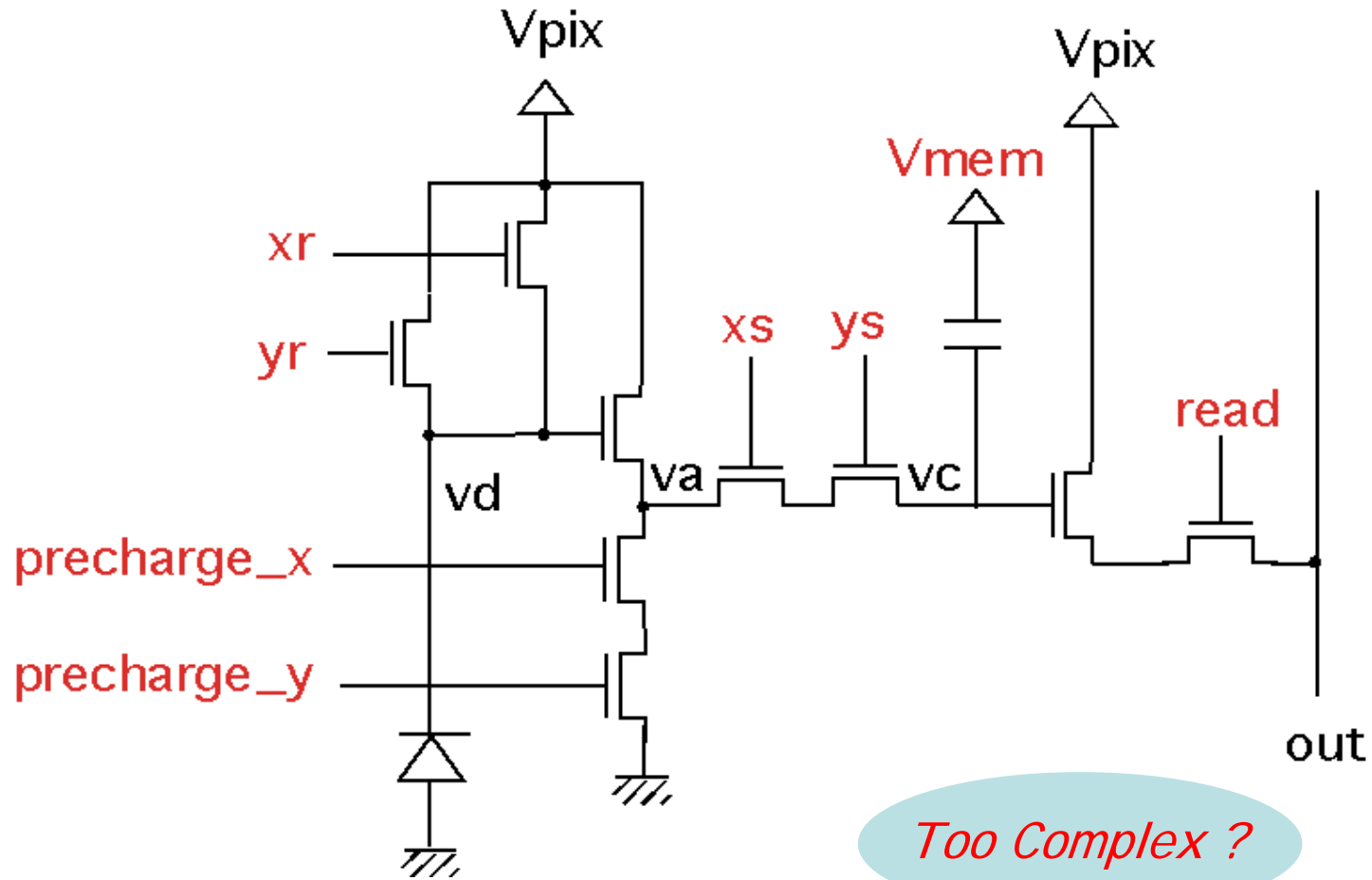


Cvd is too large !

Naive Extension of 6T cell to 2-D

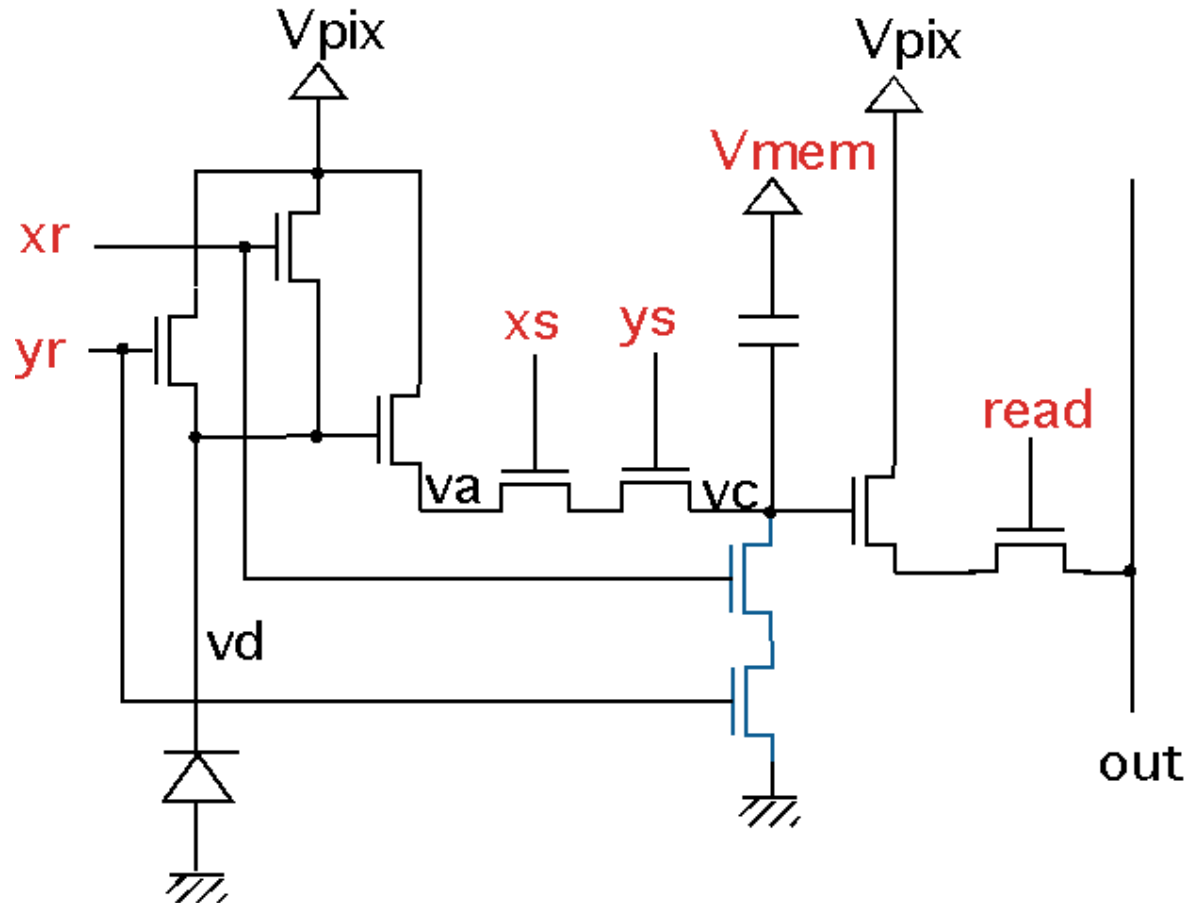
No. of Transistors : 6 -> 9 Tr

No. of Control Line : 5 -> 8 lines.

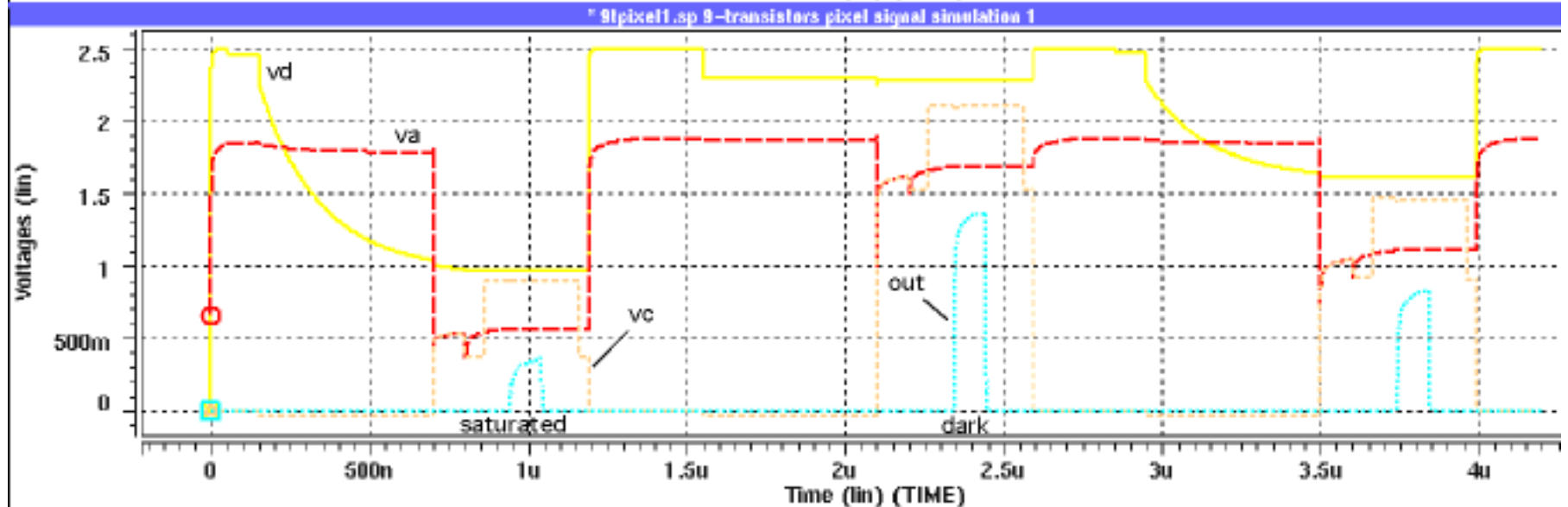
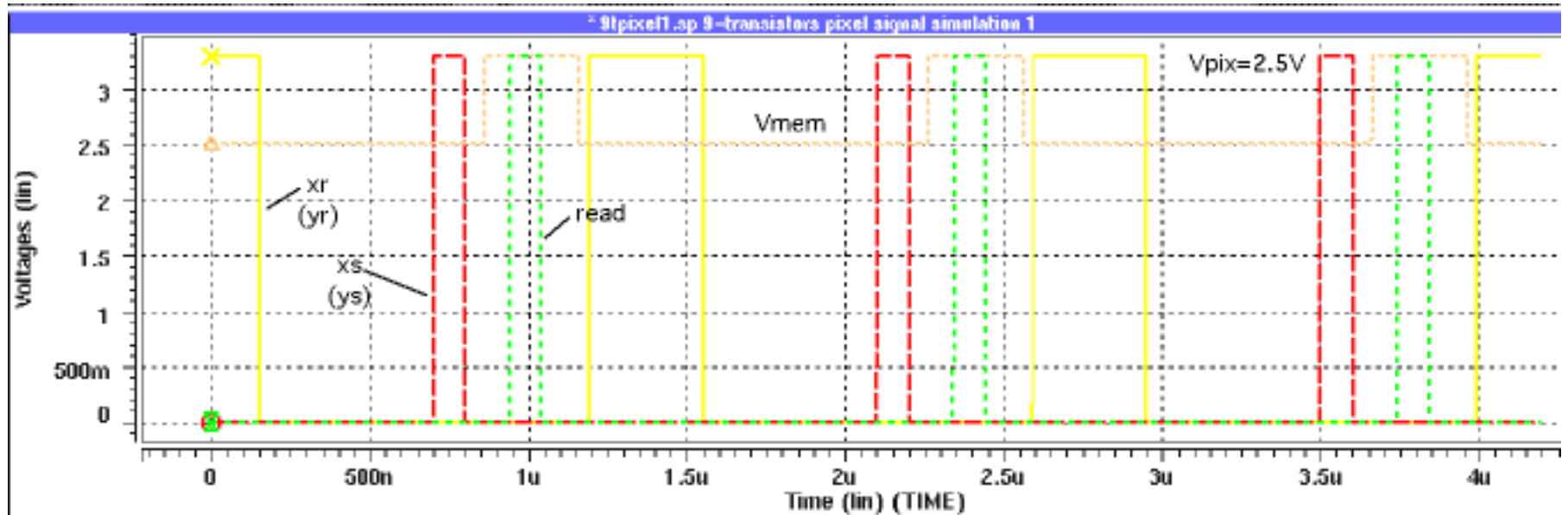


New Structure (APix-9) being investigated

No. of Transistors : 6 -> 9 Tr
No. of Control Lines : 8 -> 6 lines.

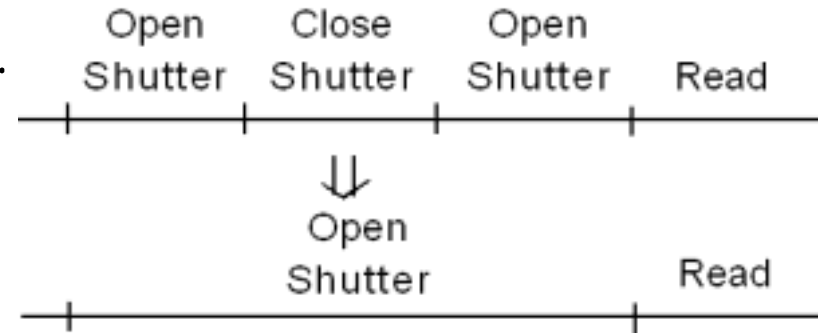


APix-9 Simulation

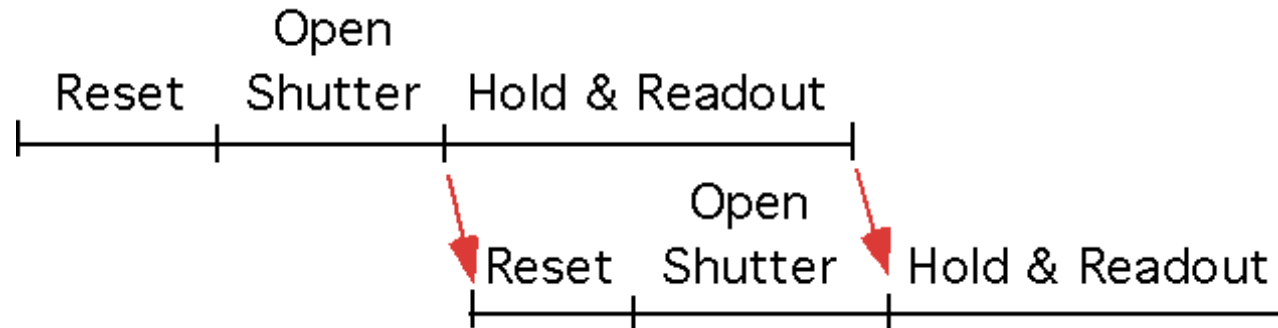


Limitation in Control

- Only continuous exposure is allowed.



- Pipeline operation is possible, but shutter must be open until previous readout is finished.



- Mirror images are generated if multiple X and Y addresses are supplied.

AFS-1 Specifications (Preliminary)

Parameter	Specification
Shutter types	2-D (128 x 128 regions, 20 pix by 20 pix, 4 pix overlap)
Readout Unit	2-D (256 x 256 regions)
Pixel size	12um x 12um
Resolution	2,048 x 2,048 pixels
Pixel rate	33 Mpix/s x 2
Conversion gain	10uV/electron@Pixel
Peak QE*FF	30% (average 25%)
Optical cross talk	< 10%
Dark Current	< 10,000 e- /sec
Noise electron	< 100 e-
Saturation charge	> 100,000 e-
Spectral sensitivity range	400 - 1000 nm
ADC	33MHz 10 bit x 2
Power dissipation	< 400 mW

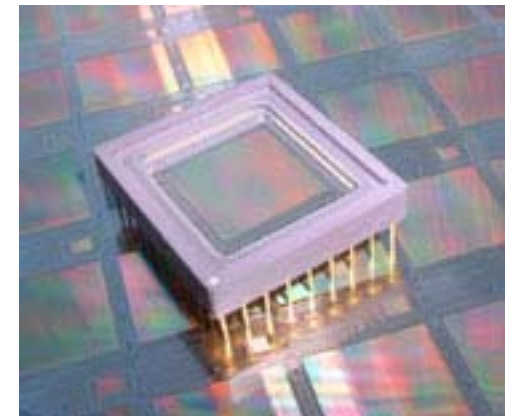
Schedule

Sensor: FillFactory

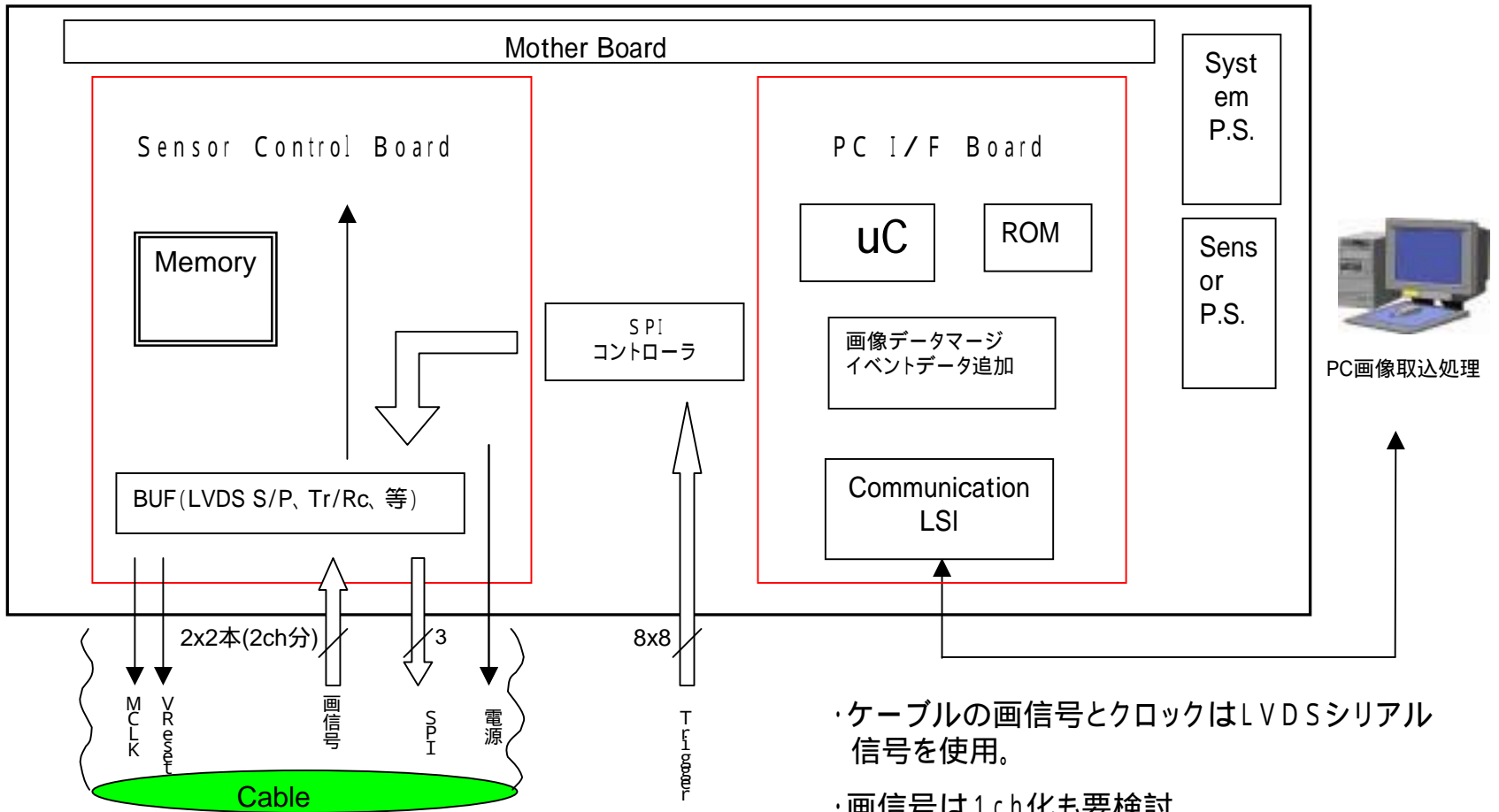
- ~Feb. 2004: Agreement on 'Statement Of Work'.
- ~Mar. 2004: Quotation and Contract.
- Fall 2004: Design finish.
- Early 2005: Sensor fabrication finish.
- Spring 2005: Evaluation finish.

Peripheral I/O: Toshiba DMS

- ~Mar. 2004: Learn FillFactory sensor control with an evaluation kit.
- ~Apr. 2004: Design and production of prototype readout modules for LUPA-4000 sensor.



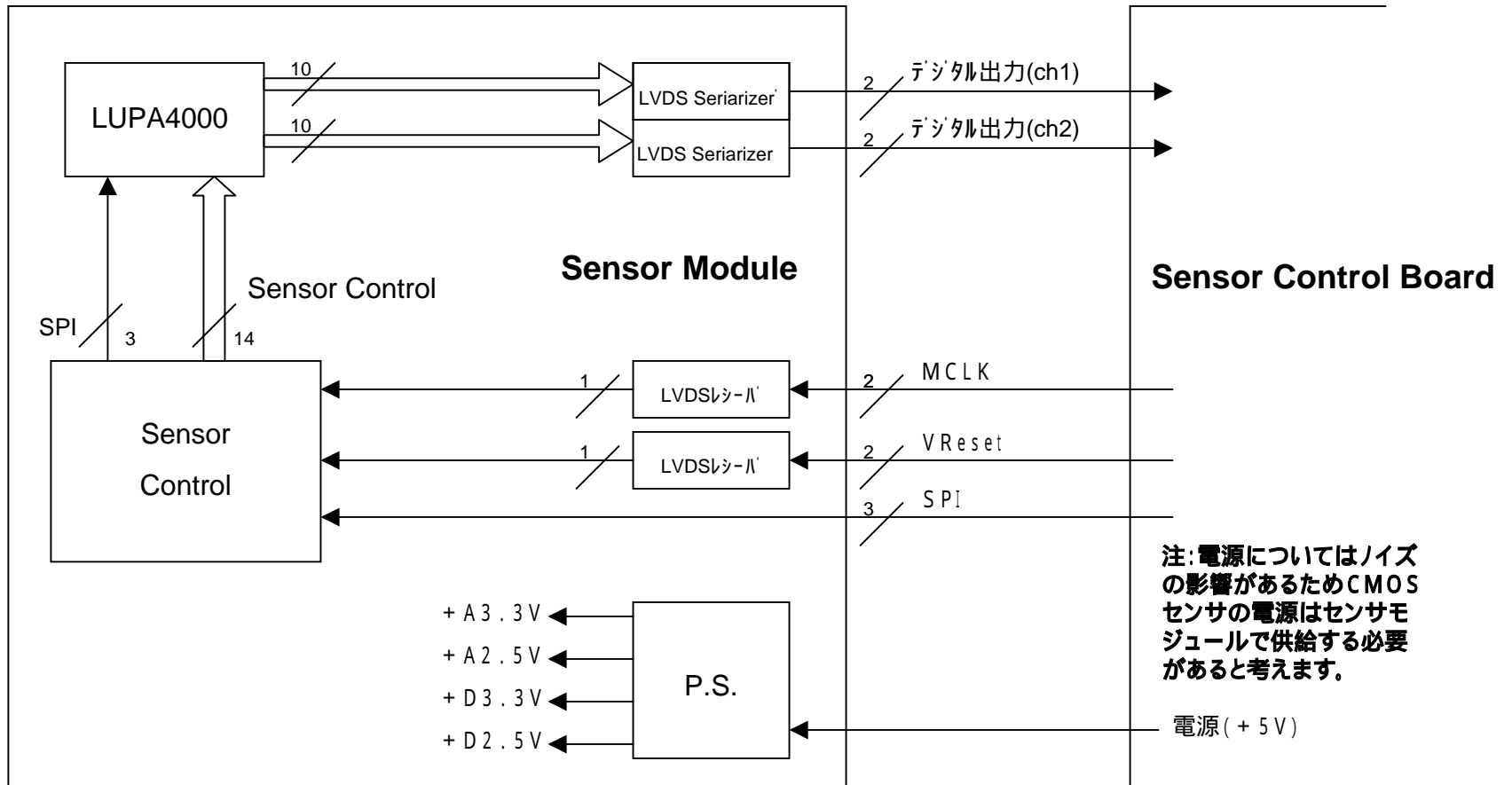
LUPA-PC I/F



To LUPA4000 Sensor Module

- ・ケーブルの画信号とクロックはLVDSシリアル信号を使用。
- ・画信号は1ch化も要検討

LUPA4000 Sensor Module



Summary

- Architecture of Ashra Fine Sensor is being studied (2,048x2,048 pixels, 2-D control of exposure and readout).
- Discussion with FillFactory for the sensor development has been started.
- Several pixel structures are studied and simulated. Present candidate is 9 Tr pixel (APix-9).
- A prototype readout module is being developed by Toshiba DMS.