

# CTA小型望遠鏡用カメラの開発

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**Solar-Terrestrial Environment Laboratory, Nagoya University**

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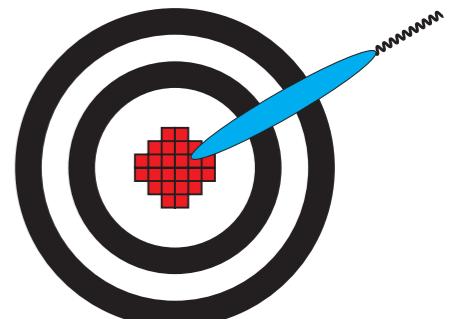
**SLAC National Accelerator Laboratory**

**Kavli Institute for Particle Astrophysics and Cosmology**

*Richard White, Jim Hinton*

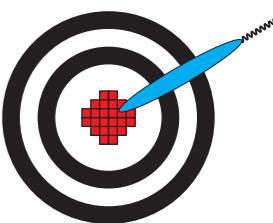
**Department of Physics and Astronomy**

**University of Leicester**

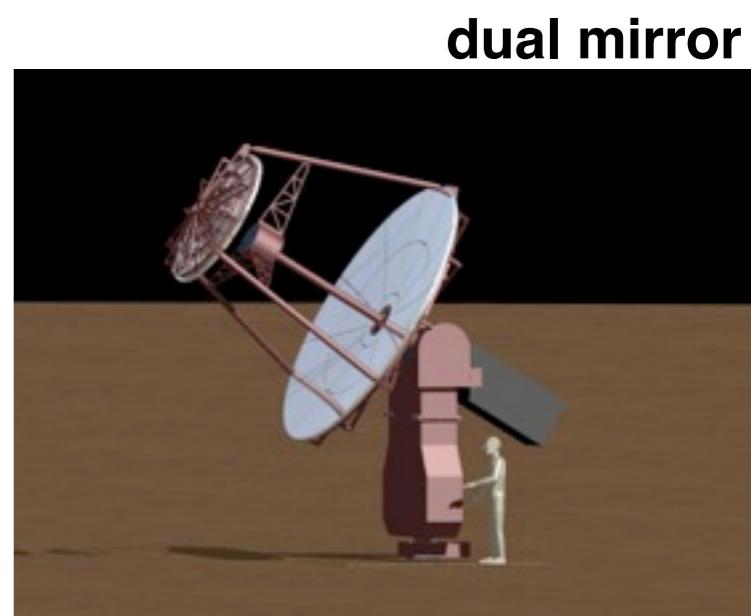
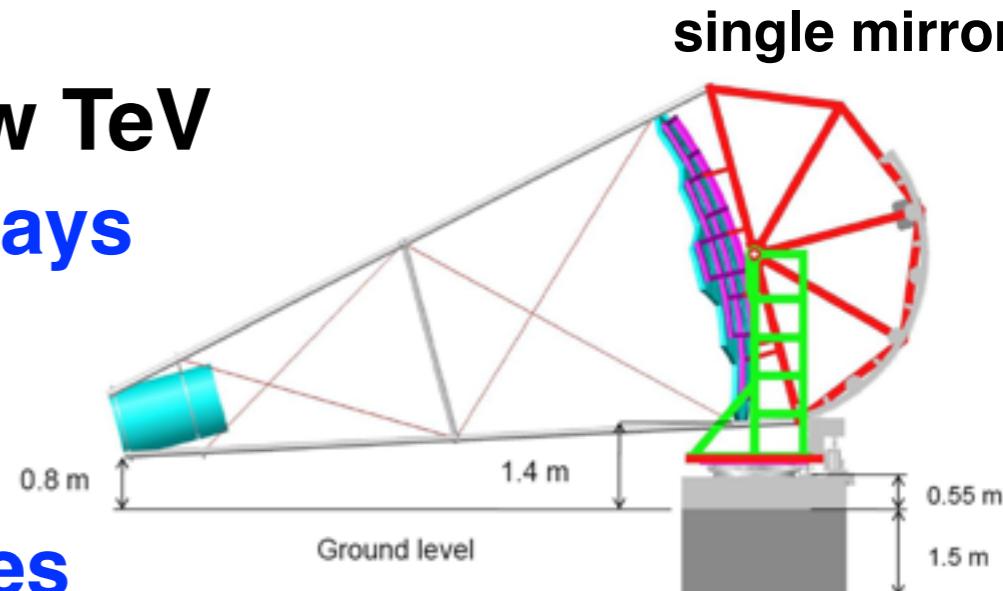


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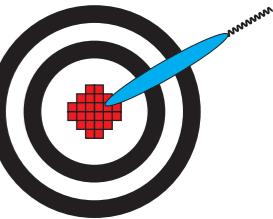
# Small-sized Telescopes (SSTs)



- ❖ CTA consist of LST, MST and SST
  - ❖ SST observes gamma rays above a few TeV
    - ✿ Flux is much lower than ~TeV gamma rays
    - ✿ Large collection area is required
- ↓
- ✿ Large number of inexpensive telescopes
    - ◆ Smaller mirrors < 6 mΦ
    - ◆ Camera cost becomes dominant
- ↓
- ✿ Development of inexpensive camera
    - ◆ Multi-channel photon sensors
      - SiPMs and MAPMTs
    - ◆ Multi-channel waveform recording ICs
      - Reduction of electric parts by integration of functionalities
    - ◆ Small pixel size requires short focal length by dual-mirror tel.



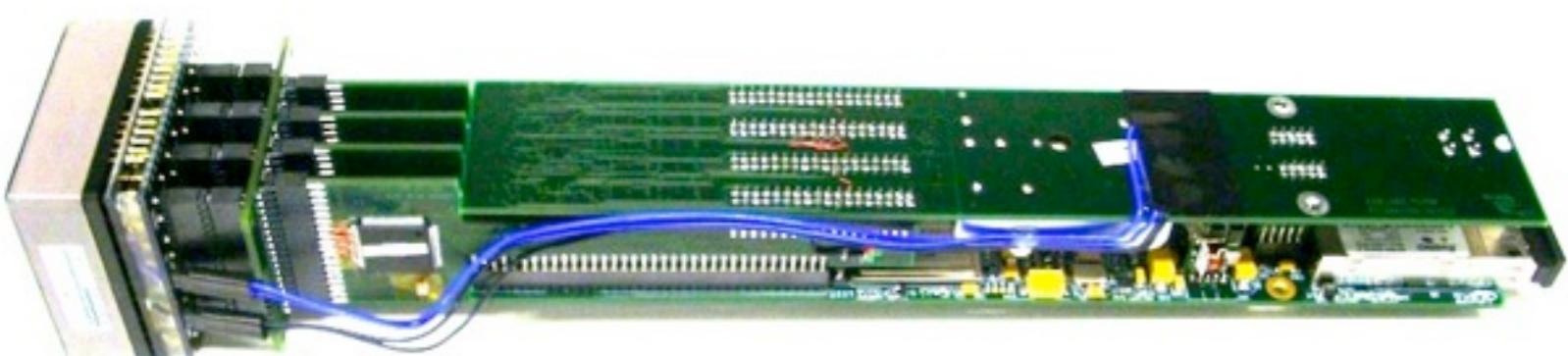
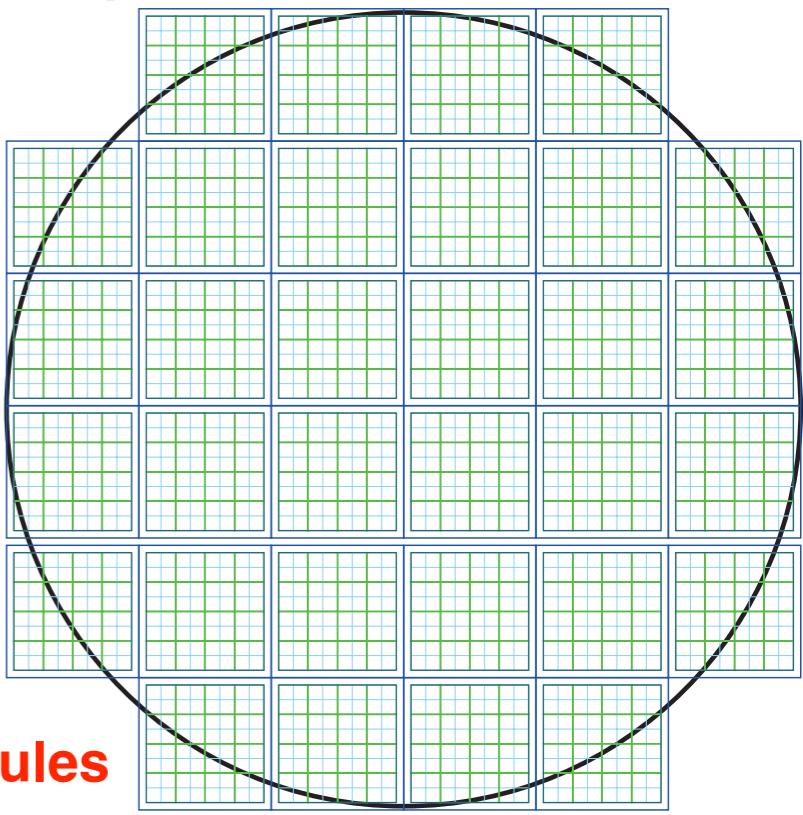
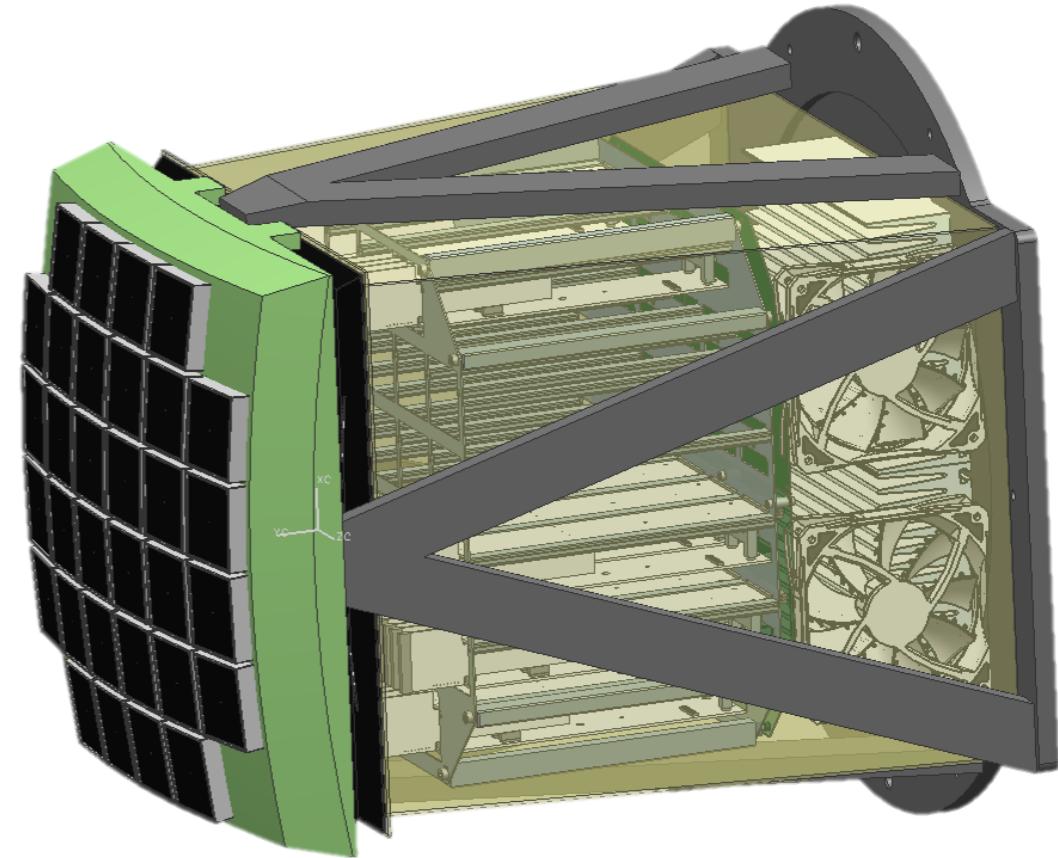
# SC-SST Camera Design

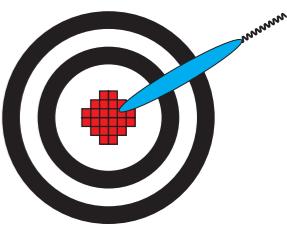


## ❖ SC-SST camera parameters

	32 mod
FOV for 0.18°/pixel (36 mm/°)	8.6°
FOV for 0.28°/pixel (23 mm/°)	13.4°
Angular pixel size for FOV=10°	0.21°
# of pixels per camera	2,048
Power consumption per camera (FE)	145 W
Weight per camera (FE+MAPMT)	11 kg
Total cost (FE+BE) for 50 CAMs*	\$2.0M

\*Assuming \$20/ch, which does not explicitly include labor for mechanical module assembly and calibrations



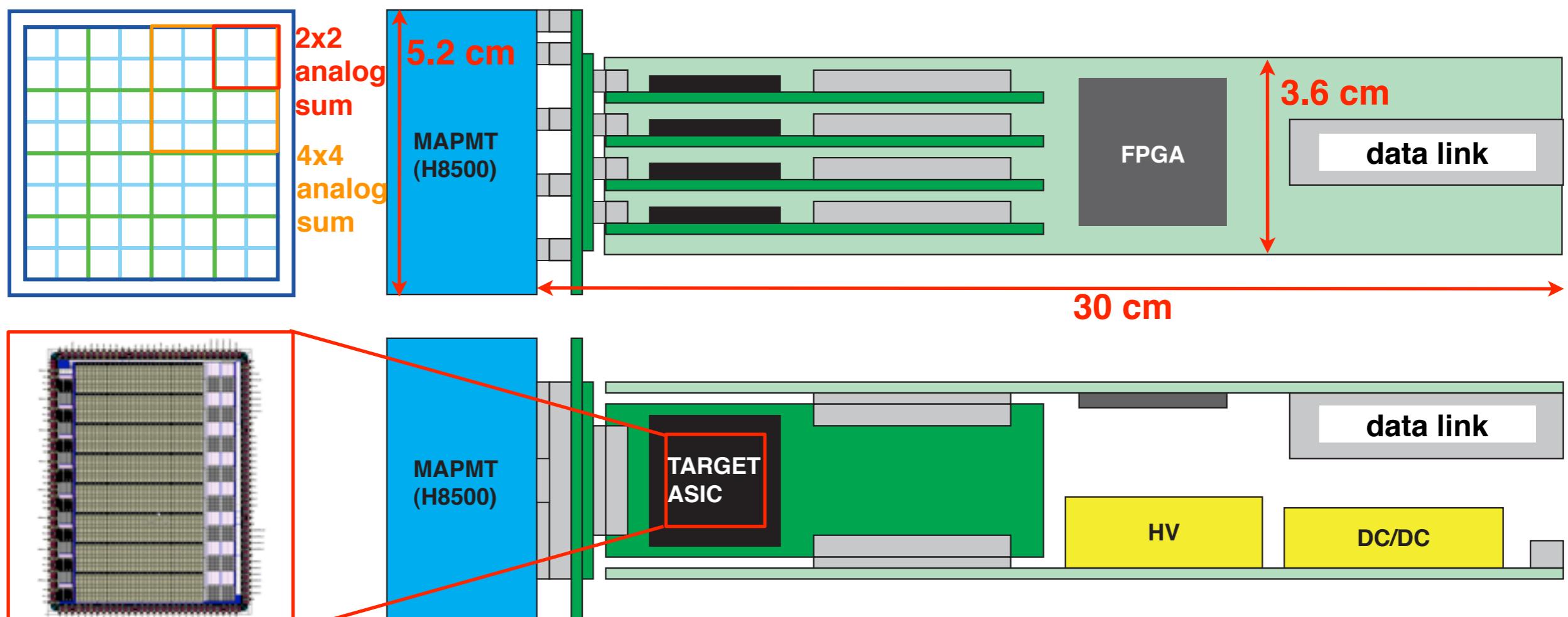


## ❖ FE (front-end) board configuration

- ❖ Sensor board (MAPMT or SiPM array, routing for 4x4 analog sum trigger)
- ❖ ASIC board (16 channels per board)
- ❖ FPGA board: FPGA, data link connector
- ❖ Power supply board: DC/DC converter, HV supply

## ❖ Minimize # of components for cost reduction and reliability

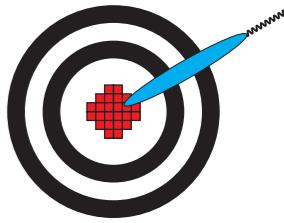
- ❖ Integration of necessary functionalities into an ASIC



designed by G. Varner  
(Hawaii)

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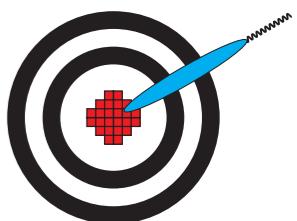
# TARGET Specifications



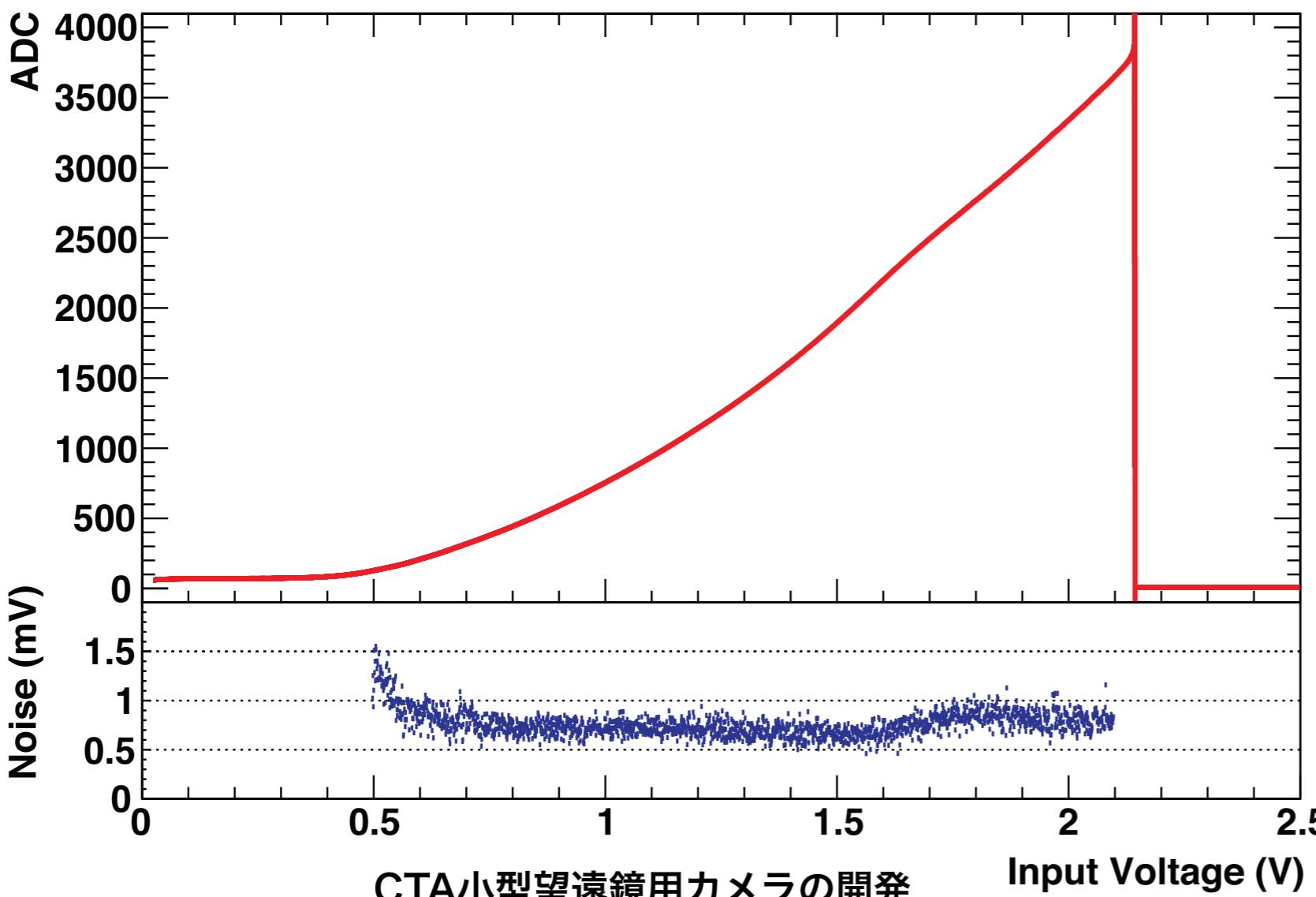
- ❖ Waveform sampling ASIC specifically designed for CTA
  - ✿ Switched capacitor array + Wilkinson-type ADC
  - ✿ Integrated trigger circuits

	TARGET-1 (measured)	TARGET-5 (expected/measured/new)
# of channels	16	16
# of cells/channel	4,096	16,384
Sampling frequency	0.5 – 2.5 GHz	0.4 – 1.2 GHz
Bandwidth	150 MHz	> 380 MHz
Crosstalk (@ -3dB)	4%	< 1%
Dynamic range	~10 bits (~1 mV/1 V)	10.5–11.2 bits (0.6–1.0 mV/1.5 V)
Digitization time	1 $\mu$ s (9 bit), 2 $\mu$ s (10bit)	1.1 $\mu$ s (10 bit), 4.6 $\mu$ s (12 bit)
# of cells/digitization	16 cells x 2 ch	32 cells x 16 ch
Data transfer speed	—	100 Mbps x 16 ch
Dead time (48 cells/ch)	10 bit 49 $\mu$ s	2.3 + 7.2 $\mu$ s
	12 bit 197 $\mu$ s	9.1 + 7.2 $\mu$ s
# of trigger output	1 (OR of 16 triggers)	4 (analog sum of 4 ch) + 1 (16 ch)

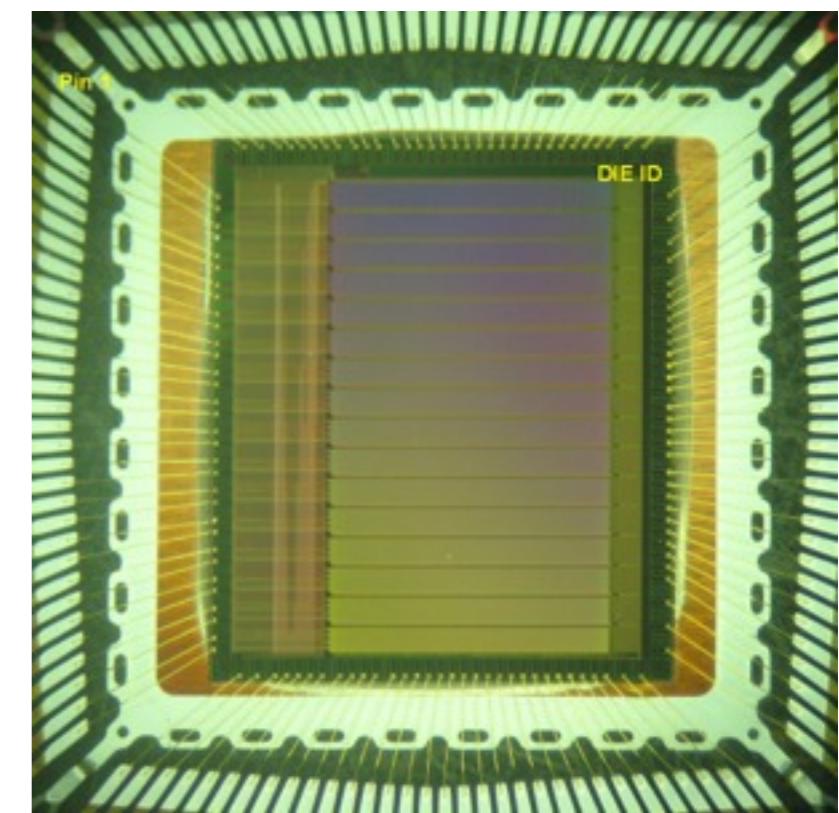
# TARGET ASIC Development Status



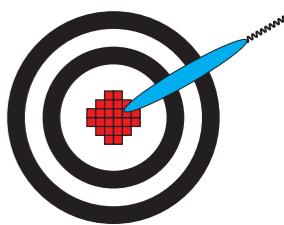
- ❖ Development of TARGET-5 to address issues found in TARGET-2
- ❖ TARGET-5 (qty. 240) was delivered to Nagoya/STEL on Aug/24
- ❖ Initial measurements indicate TARGET-5 satisfy requirements
  - ✿ Dynamic range, crosstalk, bandwidth are most critical
  - ✿ Evaluation of trigger performance in progress



**TARGET5**  
designed by Gary Varner

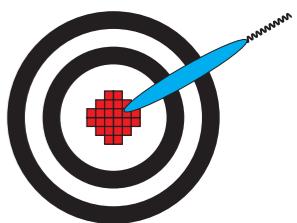


# Comparison of Photon Detectors



	MPPC(SiPM)	MAPMT	HPD	APD
Size	55 mm	52 mm	73 mm	—
Pixel size	6.0 mm	6.1 mm	4.9 mm	—
# of pixels	8x8	8x8	12x12	—
aperture ratio	69–76%	89%	64%	—
Q.E. (peak)	65% <span style="border: 2px solid red; padding: 2px;"> </span>	27–35%	32%	85%
peak wavelength	450 nm	340–380 nm	360 nm	~800 nm
Gain	$\sim 10^6$	$10^4\text{--}10^6$	$10^4\text{--}10^5$	10–100
HV	30–70 V	1–2 kV	8 kV	100–500 V
Timing	30 ps	~100 ps	~100 ps	~ 1 ns
Cost (kJPY)	125 <span style="border: 2px solid red; padding: 2px;"> </span>	138		—
Dynamic range	$\sim 10^3$	$\sim 10^6$	$>10^5$	—
Dark noise rate	$10^3\text{--}10^6$ Hz			—

# Calculation of Cherenkov Light Yield

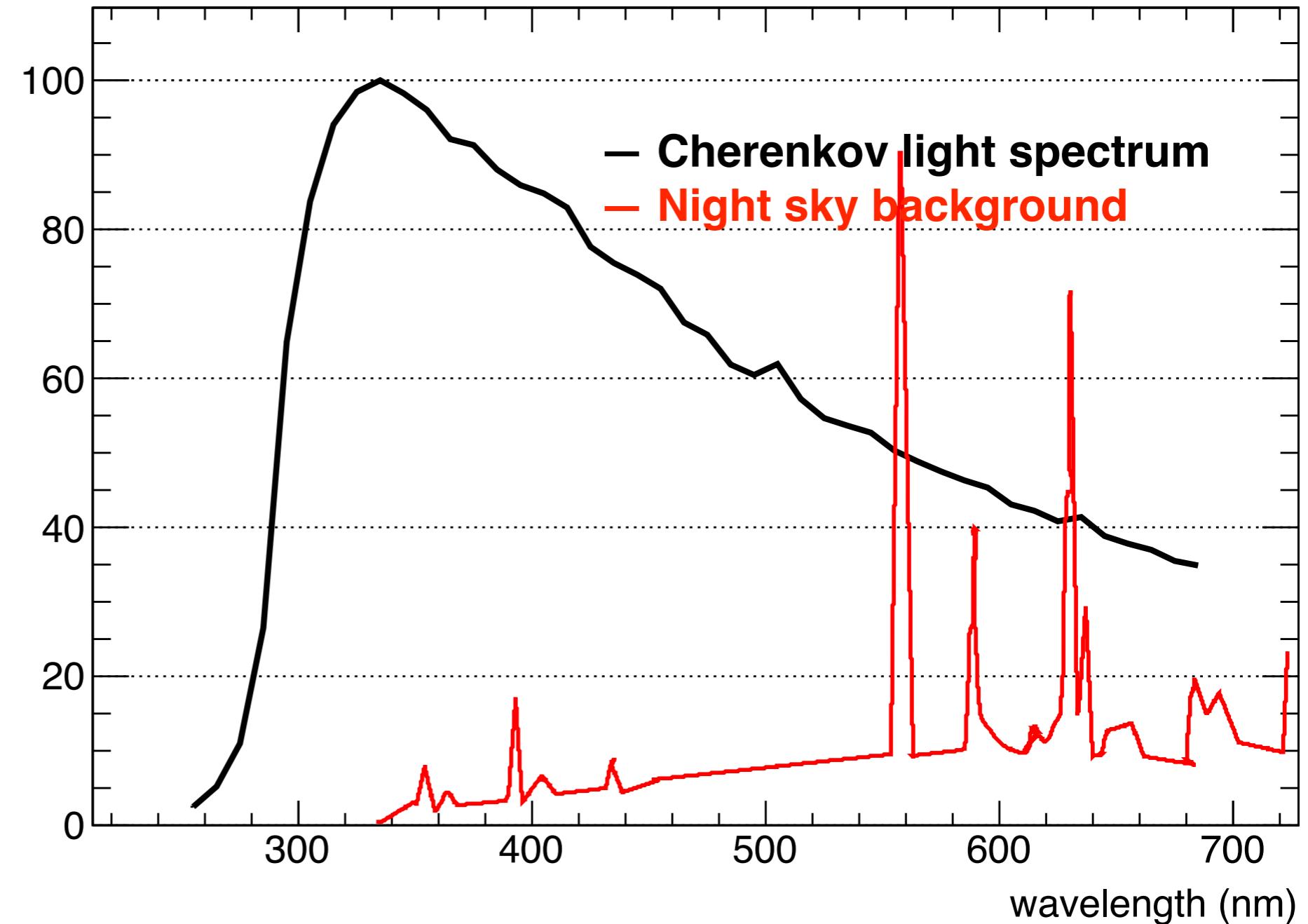


- ❖ Integrate Cherenkov light spectrum weighted by photon detection efficiency up to 550 nm

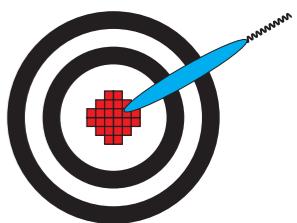
❖ Avoid Oxygen fluorescent line

❖ MPPC PDE  
from catalog

❖ MAPMT PDE  
from MPPC PDE  
and PDE ratio



# Calculation of Cherenkov Light Yield



- ❖ Integrate Cherenkov light spectrum weighted by photon detection efficiency up to 550 nm

- ❖ Avoid Oxygen fluorescent line

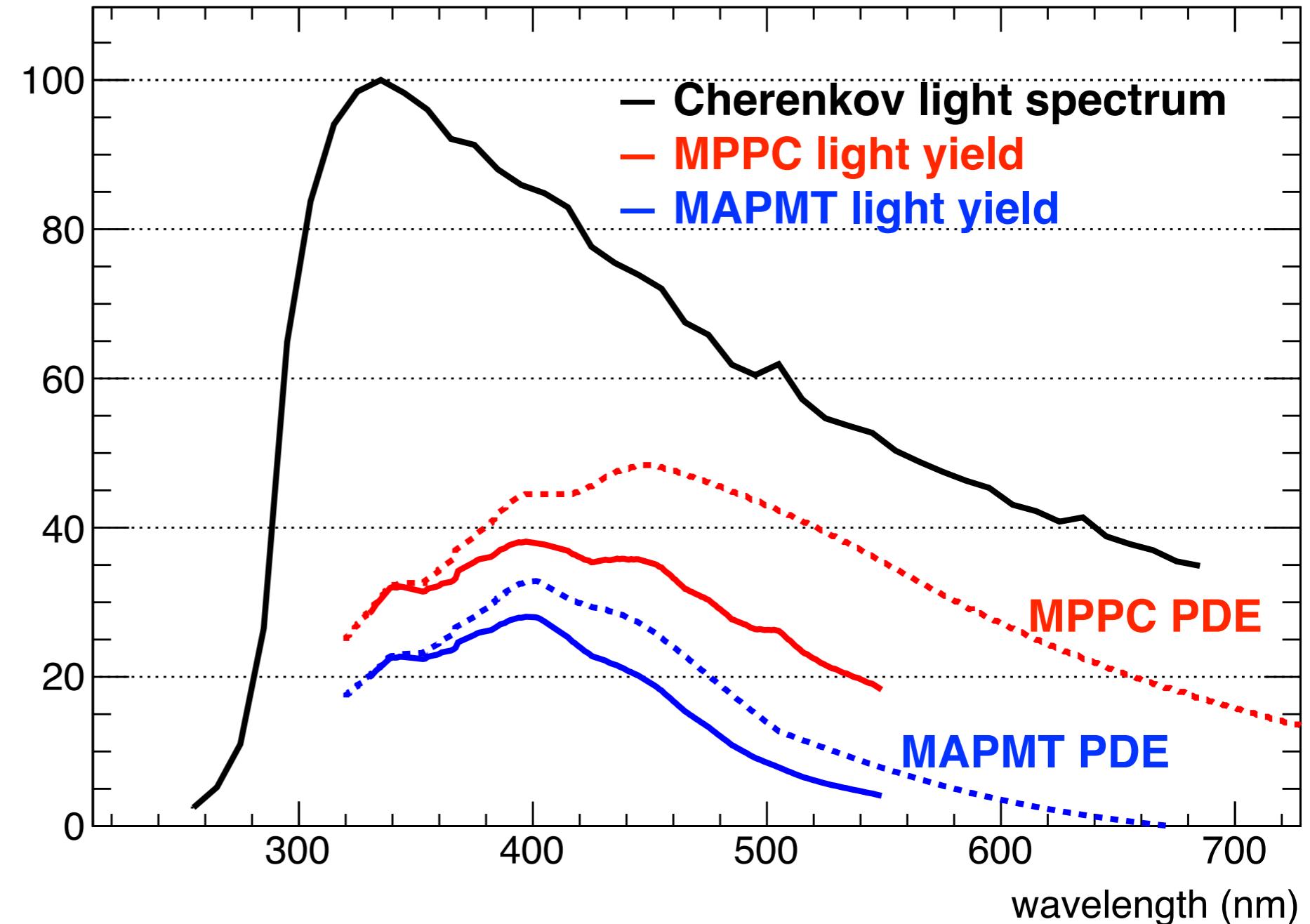
- ❖ MPPC PDE

- from catalog

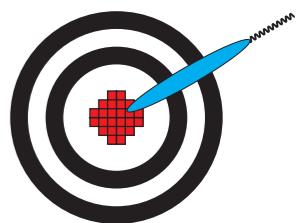
- ❖ MAPMT PDE

- from MPPC PDE

- and PDE ratio



# Calculation of Cherenkov Light Yield



- ❖ Integrate Cherenkov light spectrum weighted by photon detection efficiency up to 550 nm

❖ Avoid Oxygen fluorescent line

❖ MPPC PDE

from catalog

❖ MAPMT PDE

from MPPC PDE

and PDE ratio

$$LY(MPPC)/LY(MAPMT) = 1.77$$

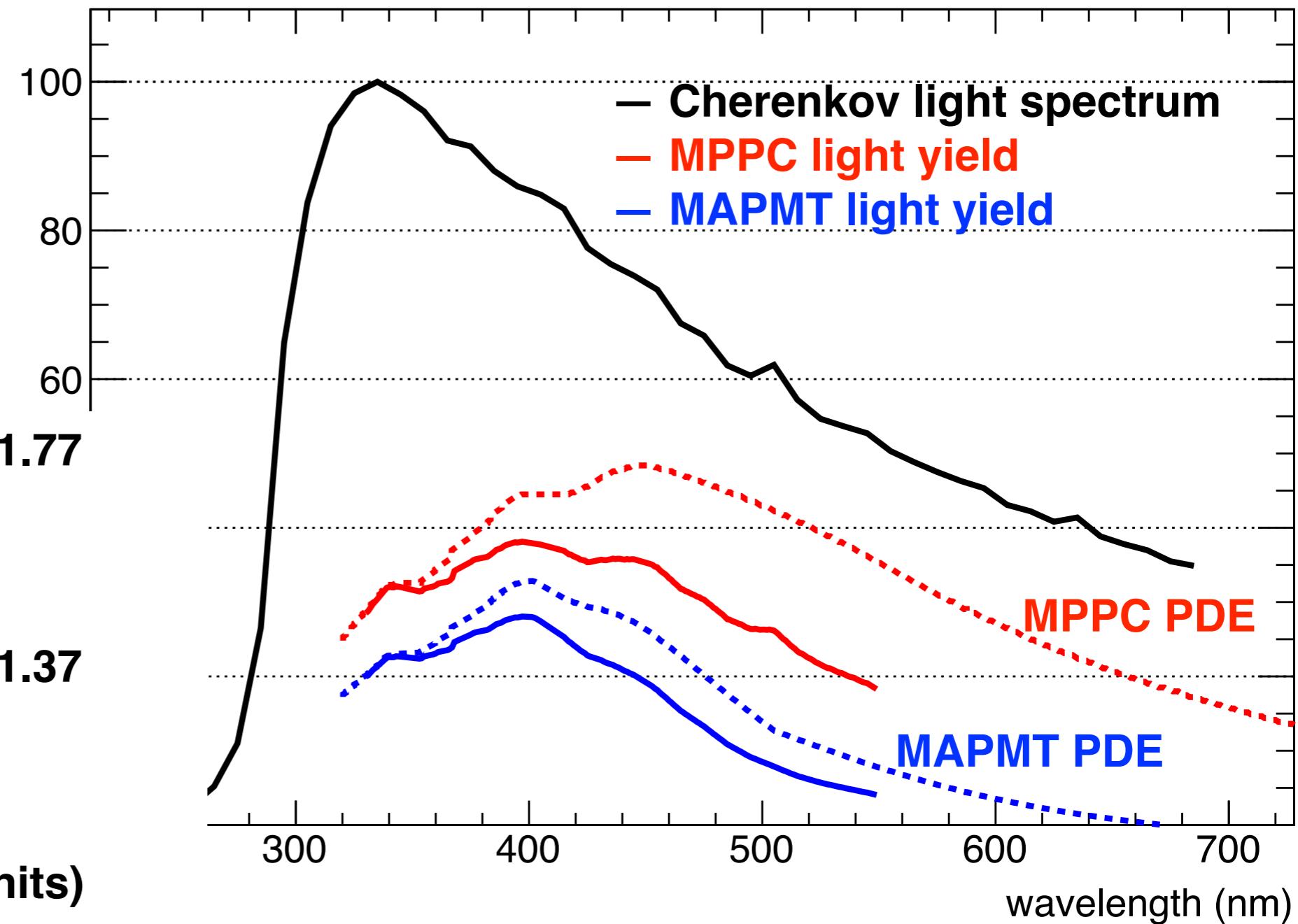
Correcting light loss at boundary of each unit

$$LY(MPPC)/LY(MAPMT) = 1.37$$

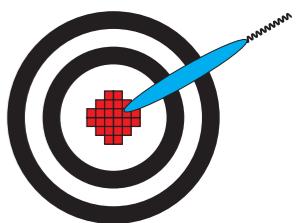
$$\epsilon(MAPMT) = 89\%$$

$$\epsilon(MPPC) = 69\%$$

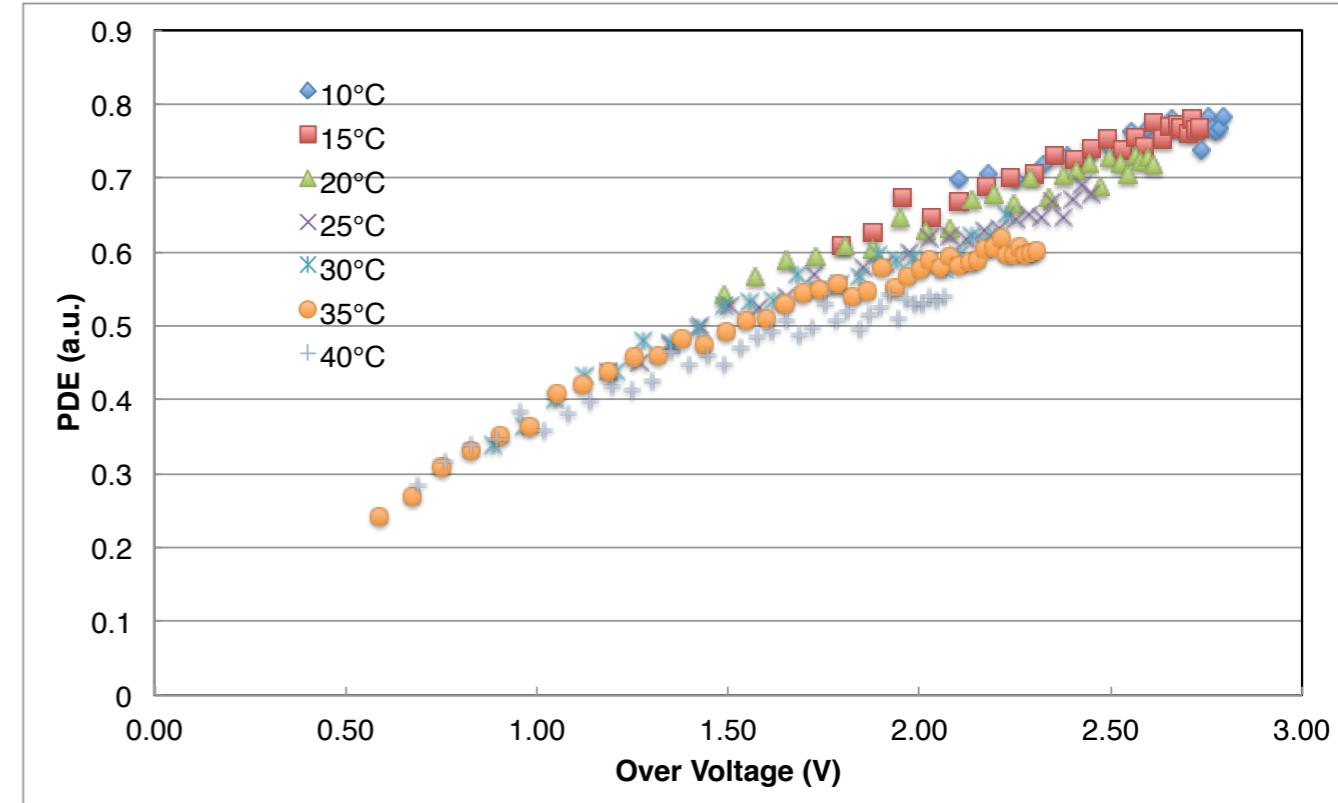
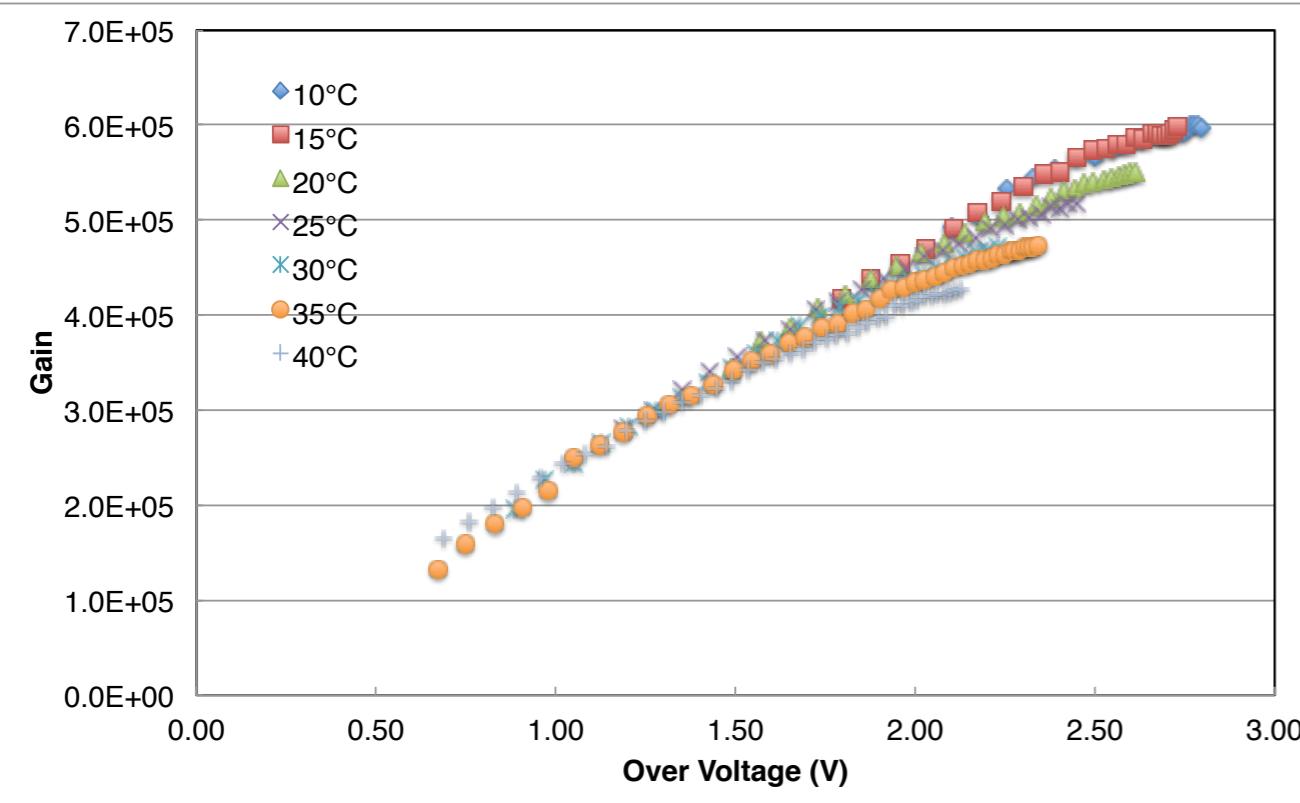
(0.5 mm gap between units)

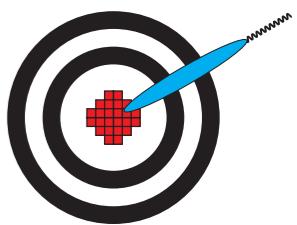


# SiPM Characterization



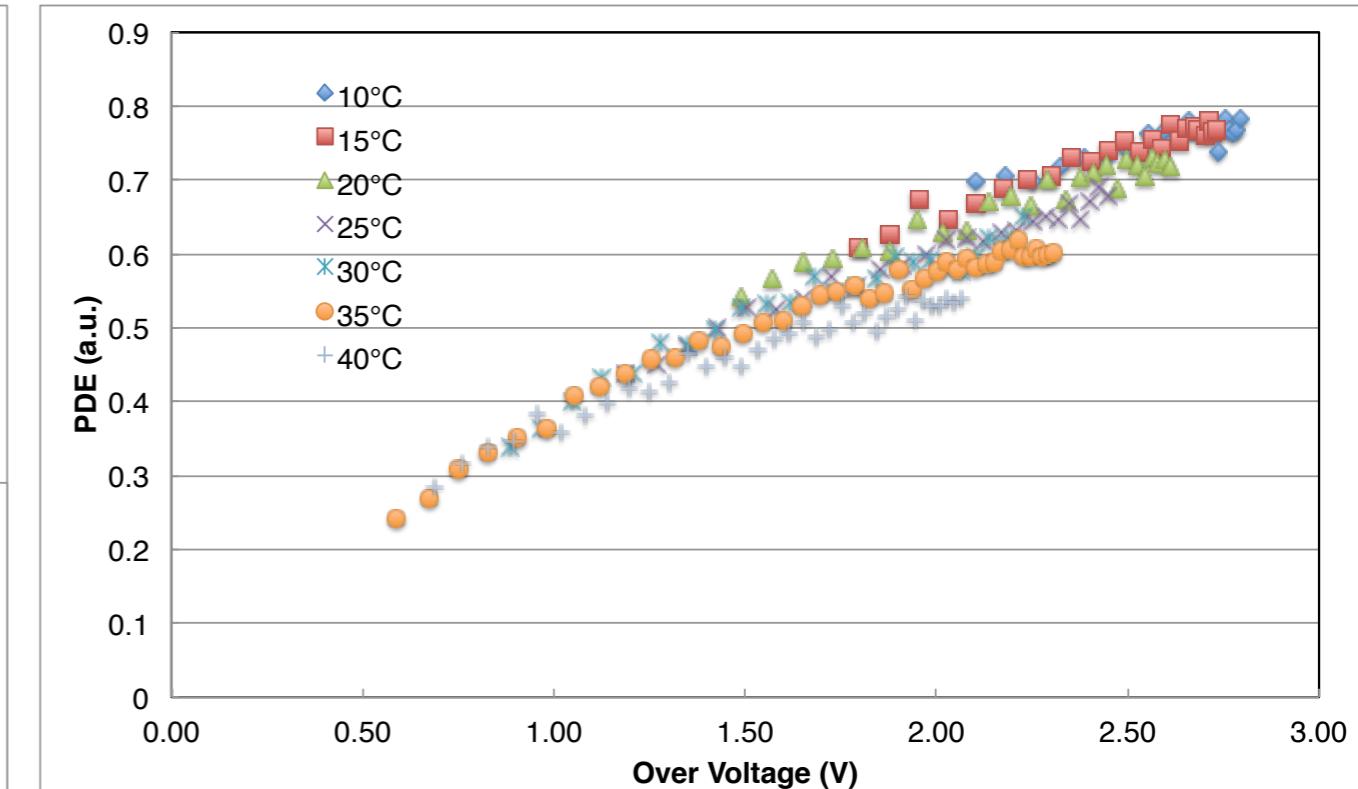
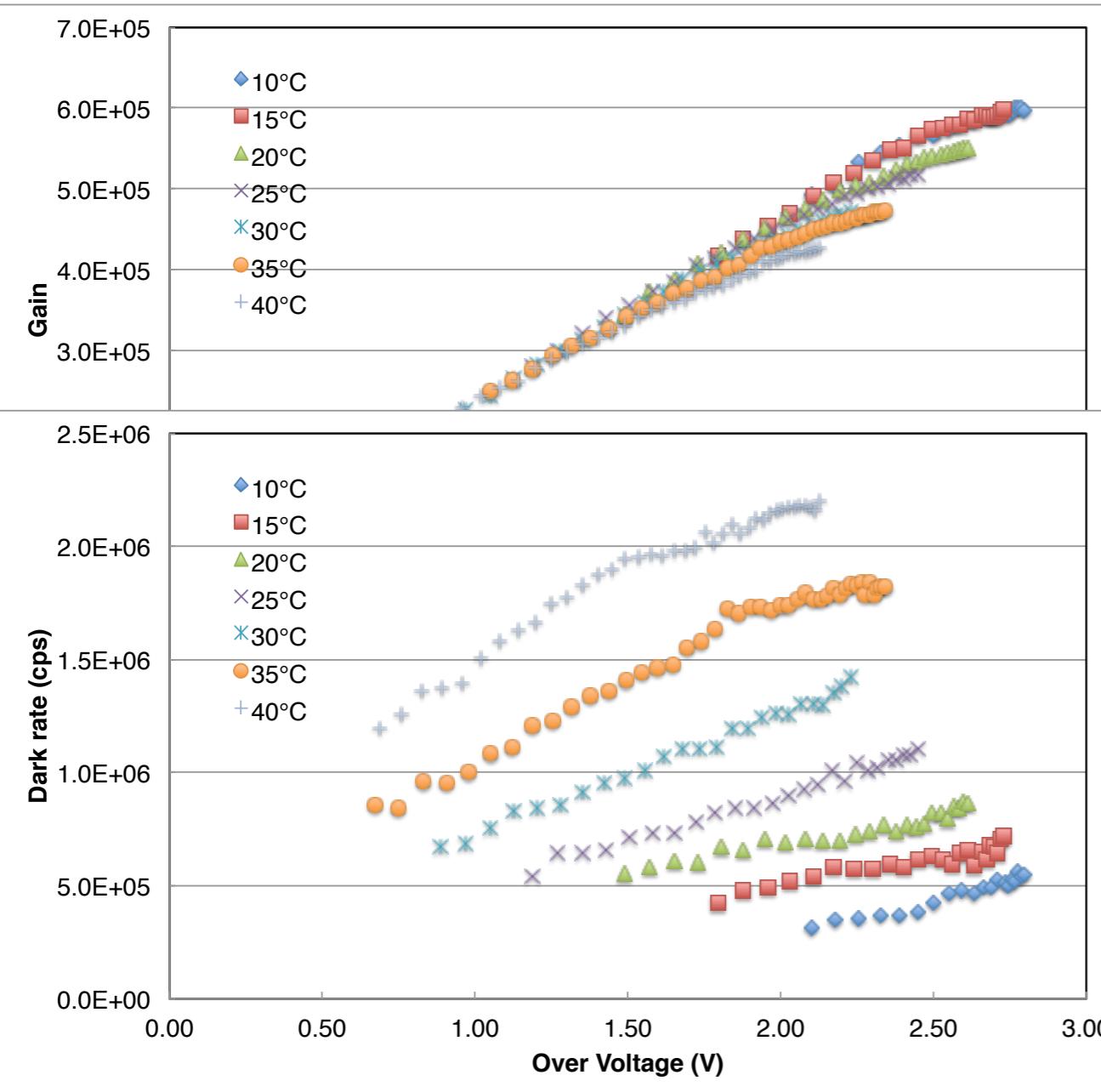
- ❖ **MPPC (Multi-Pixel Photon Counter) by HPK**
- ❖ **Characterize performance under possible conditions**
- ❖ **Study requirements on camera temperature control**



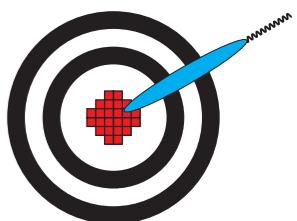


## ❖ MPPC (Multi-Pixel Photon Counter) by HPK

- ❖ Characterize performance under possible conditions
- ❖ Study requirements on camera temperature control

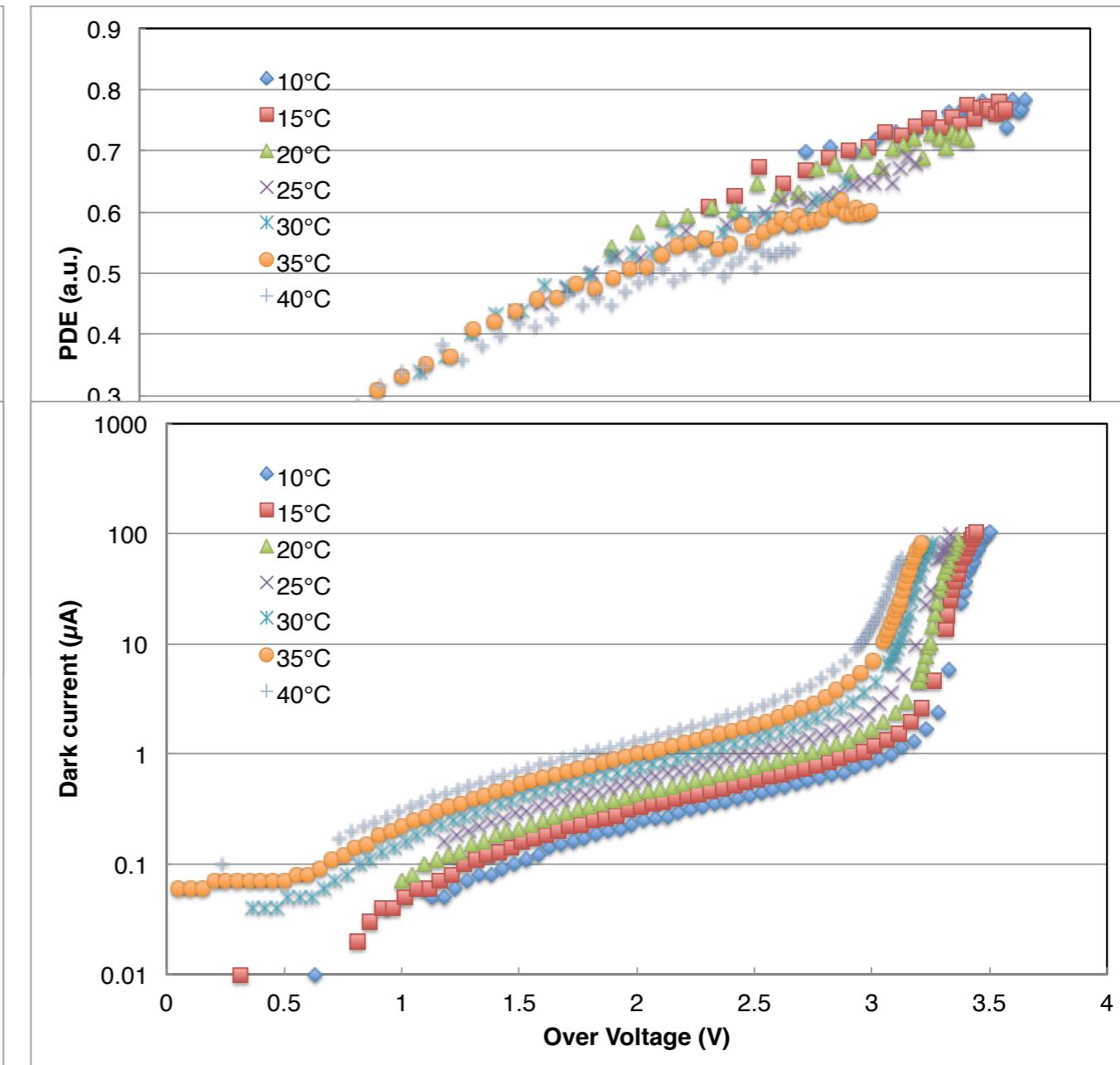
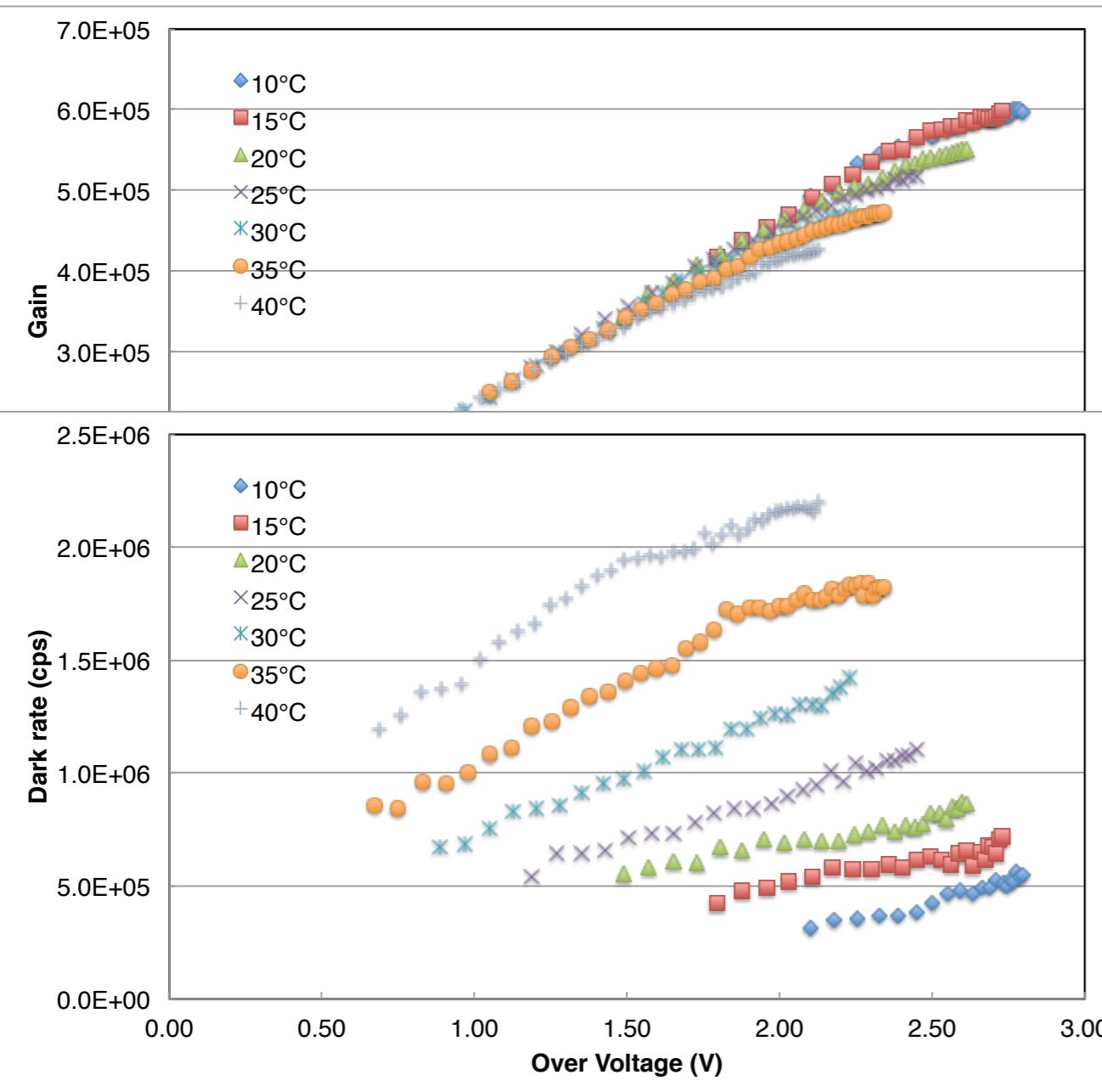


# SiPM Characterization

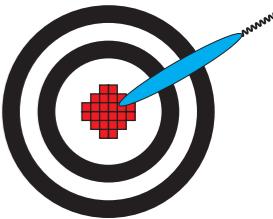


## ❖ MPPC (Multi-Pixel Photon Counter) by HPK

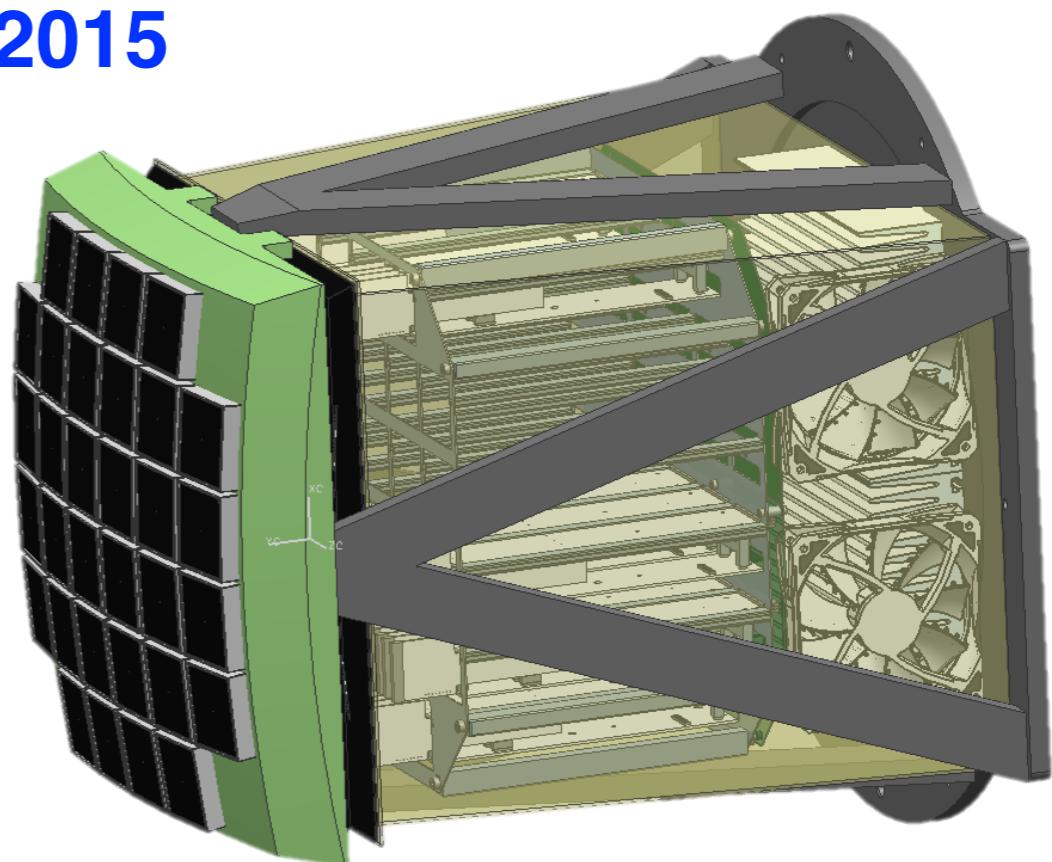
- ❖ Characterize performance under possible conditions
- ❖ Study requirements on camera temperature control



# Summary

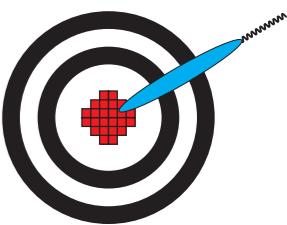


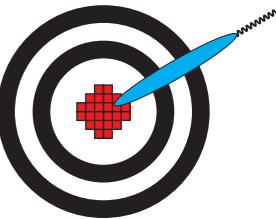
- ❖ Making good progress in TARGET ASIC development
  - ✿ Trigger performance needs adjustments
- ❖ MPPC performance being characterized
  - ✿ Cooling may be required to maximize photon detection eff.
- ❖ Fabrication of a complete prototype of MPPC SST camera by late 2014
  - ✿ to be mounted on prototype SSTs in 2015



# Supplemental slides

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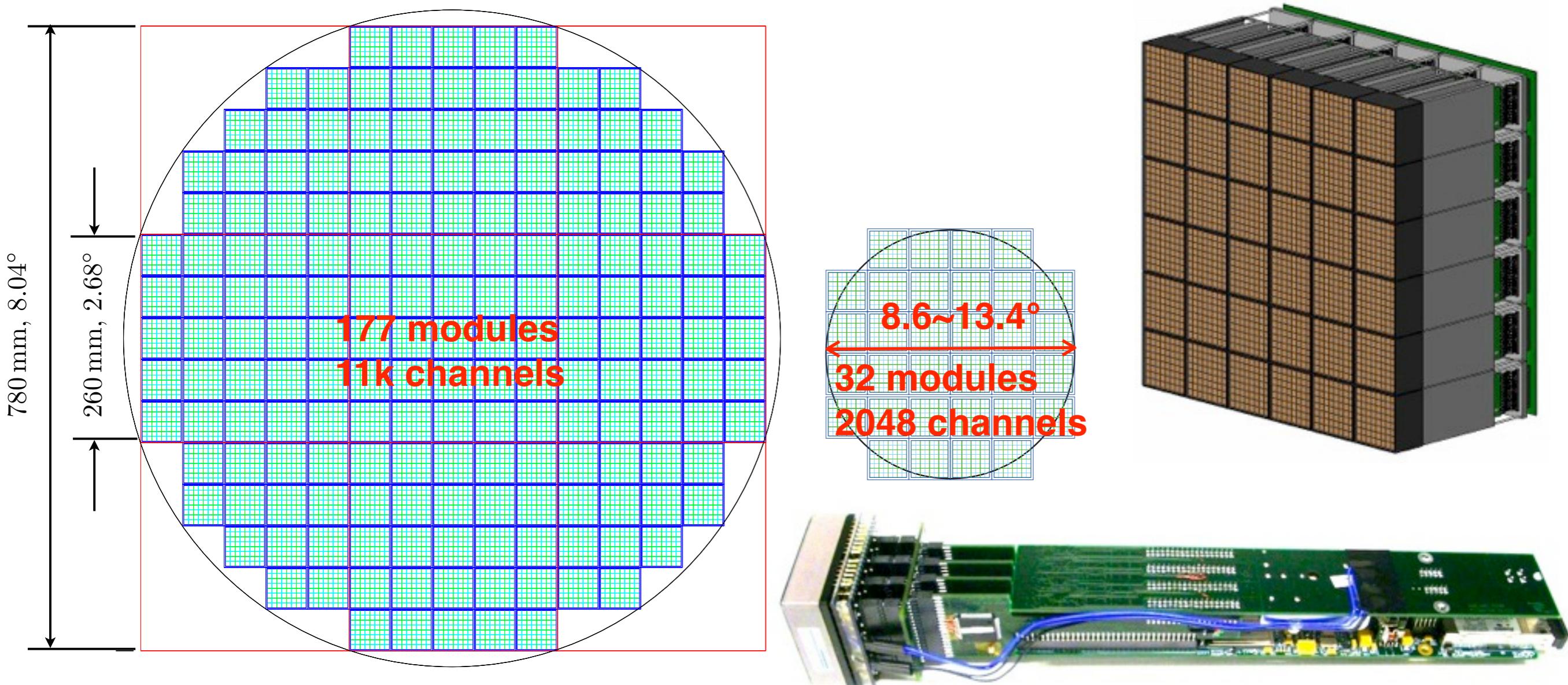


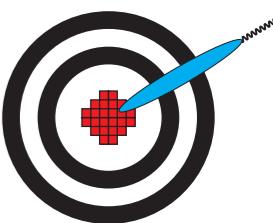


## ❖ Modular camera design

### ✿ Divided into subfields

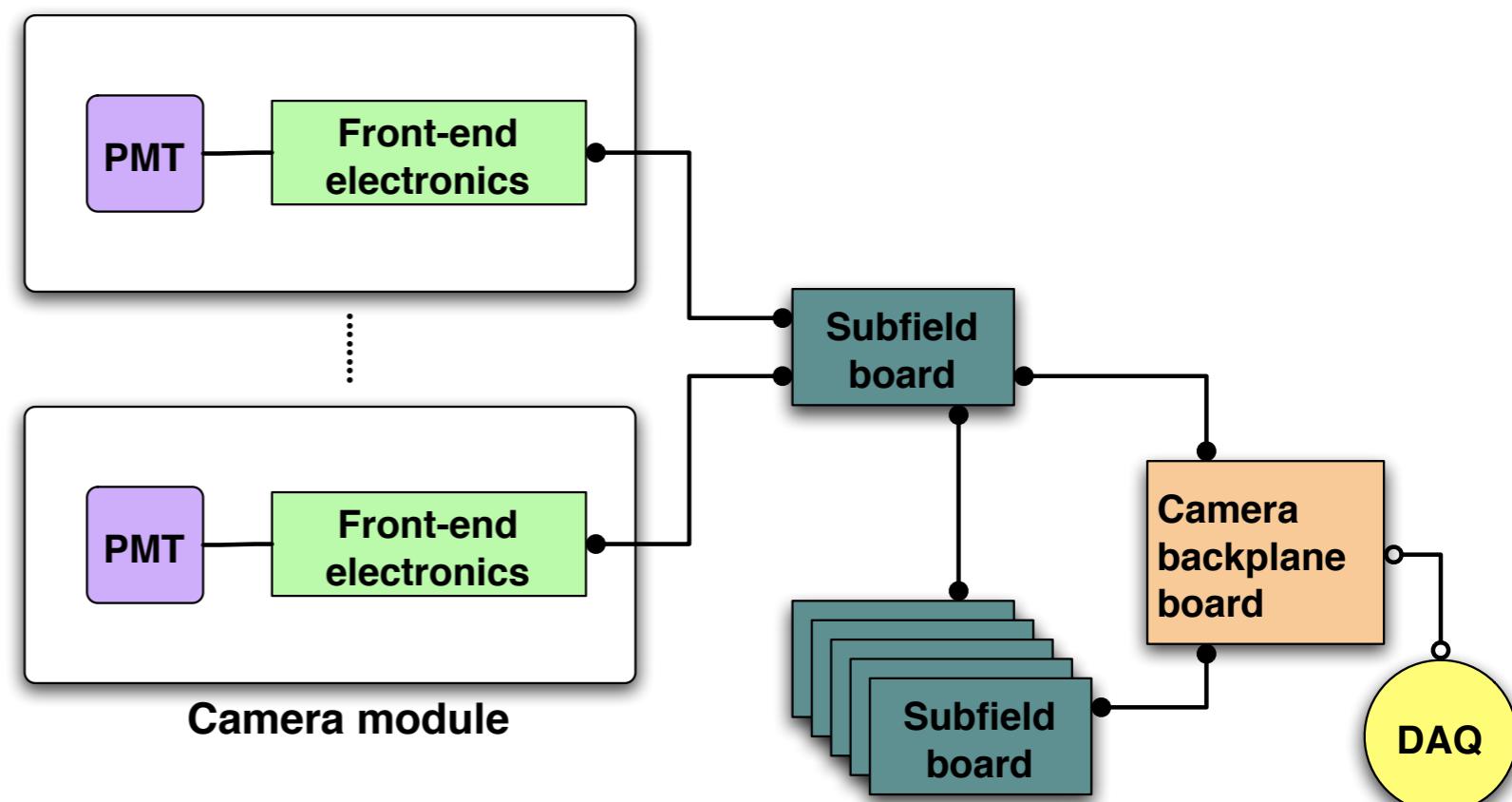
- ◆ Logical unit for trigger generation, easy maintenance



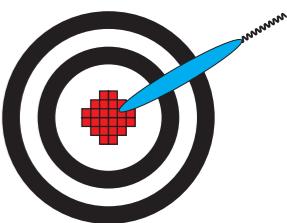


## ❖ SC-MST Camera electronics consists of

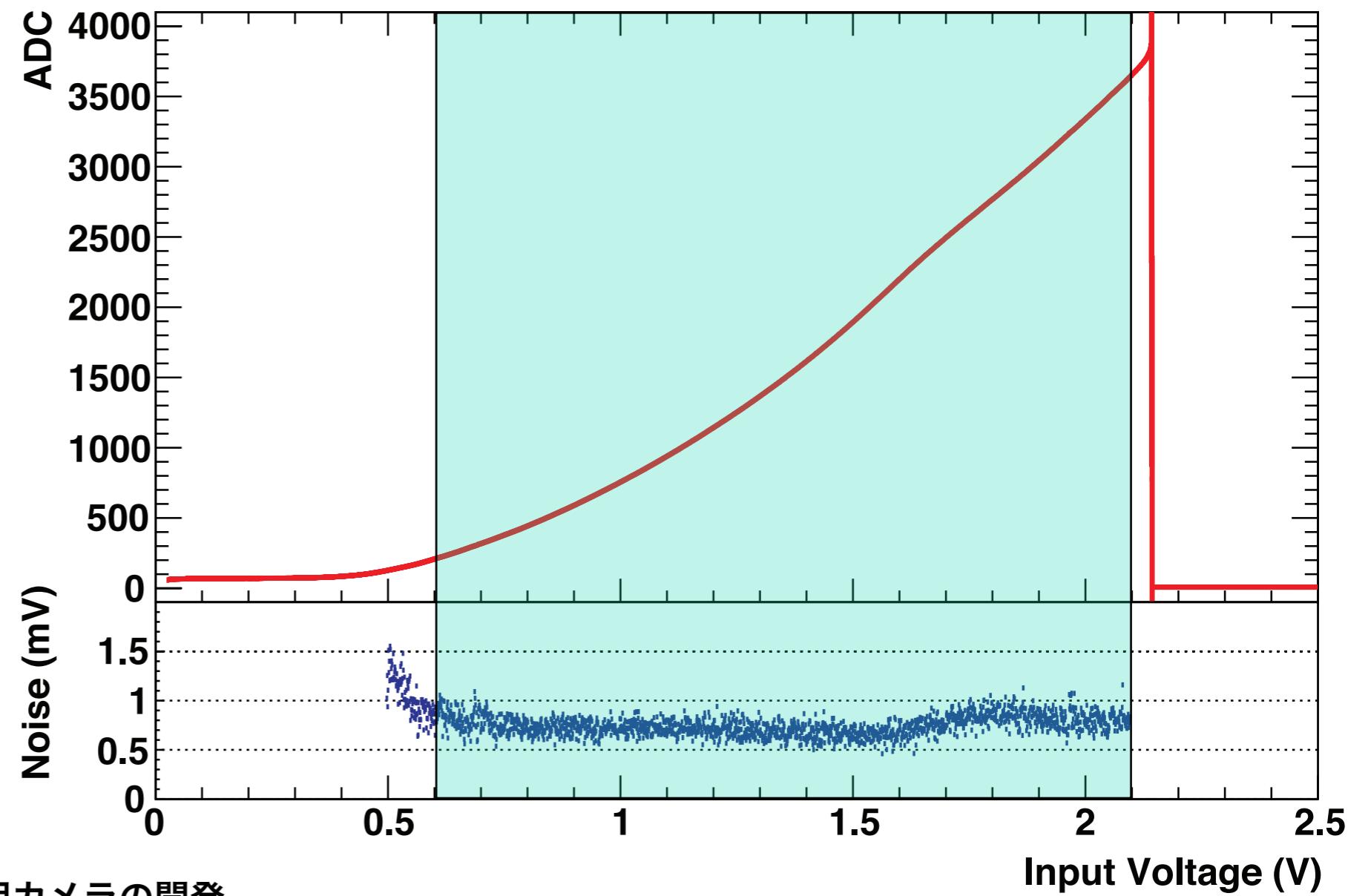
- ✿ **Camera modules: ~180/camera (~11k pixels)**
  - ◆ 64-channel PMT/GAPD + front-end electronics
  - ◆ Waveform sampling and digitization, 16 triggers
- ✿ **Subfield boards: 9/camera (25 modules/board)**
  - ◆ Cross-link trigger information
  - ◆ Subfield trigger
- ✿ **Camera backplane**
  - ◆ Camera trigger
  - ◆ Gb ethernet link to DAQ  
(or any other commercial solution)



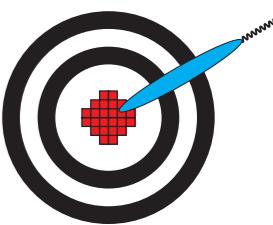
# Dynamic Range



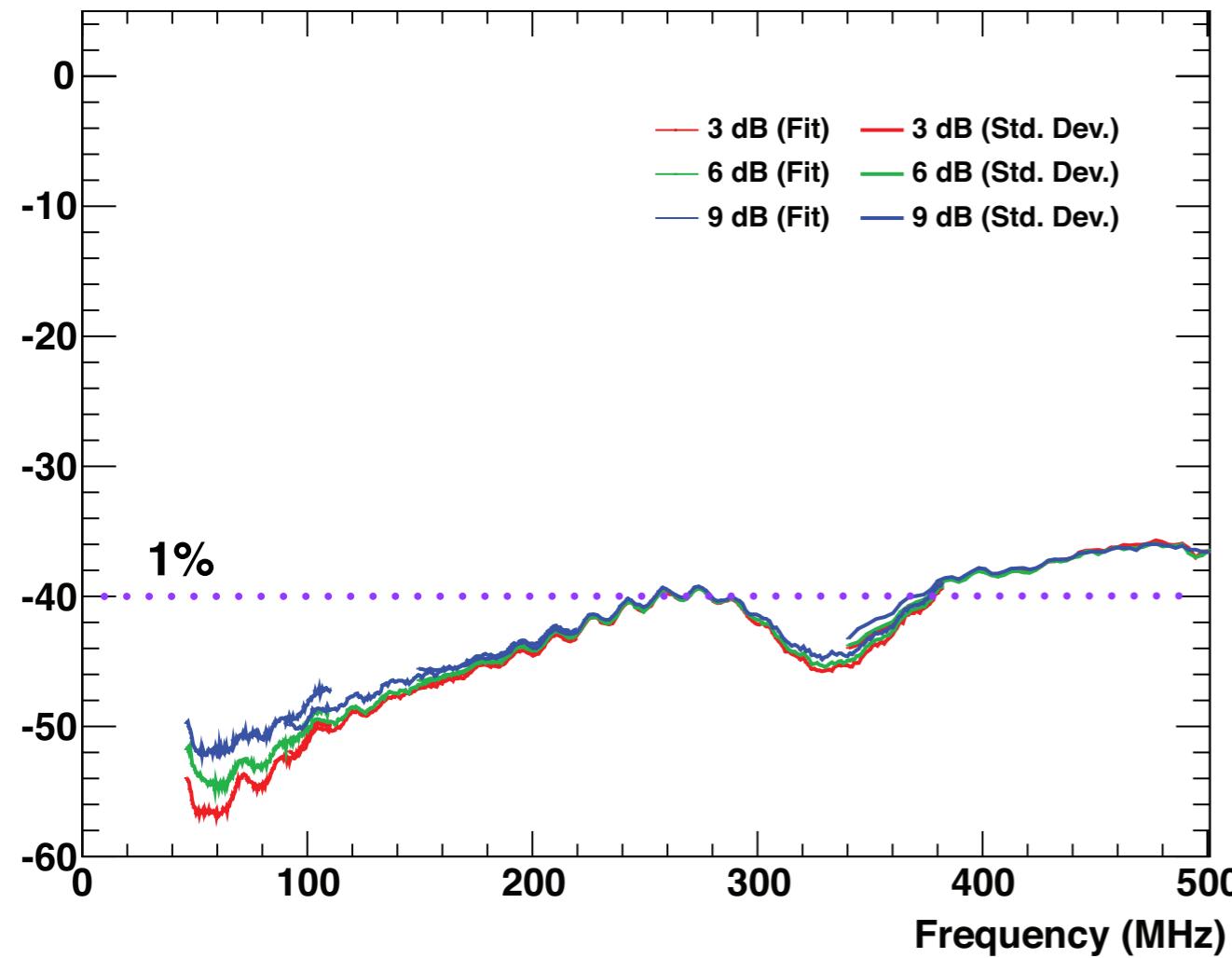
- ❖ Input voltage range: 0.6 – 2.1 V
- ❖ Noise: 0.6 – 1.0 mV
- ❖ Dynamic range:  $1.5 \text{ V}/(0.6 - 1.0 \text{ mV}) = 10.5 - 11.2 \text{ bits}$
- ✿ Better noise at lower voltage prefers positive pulse



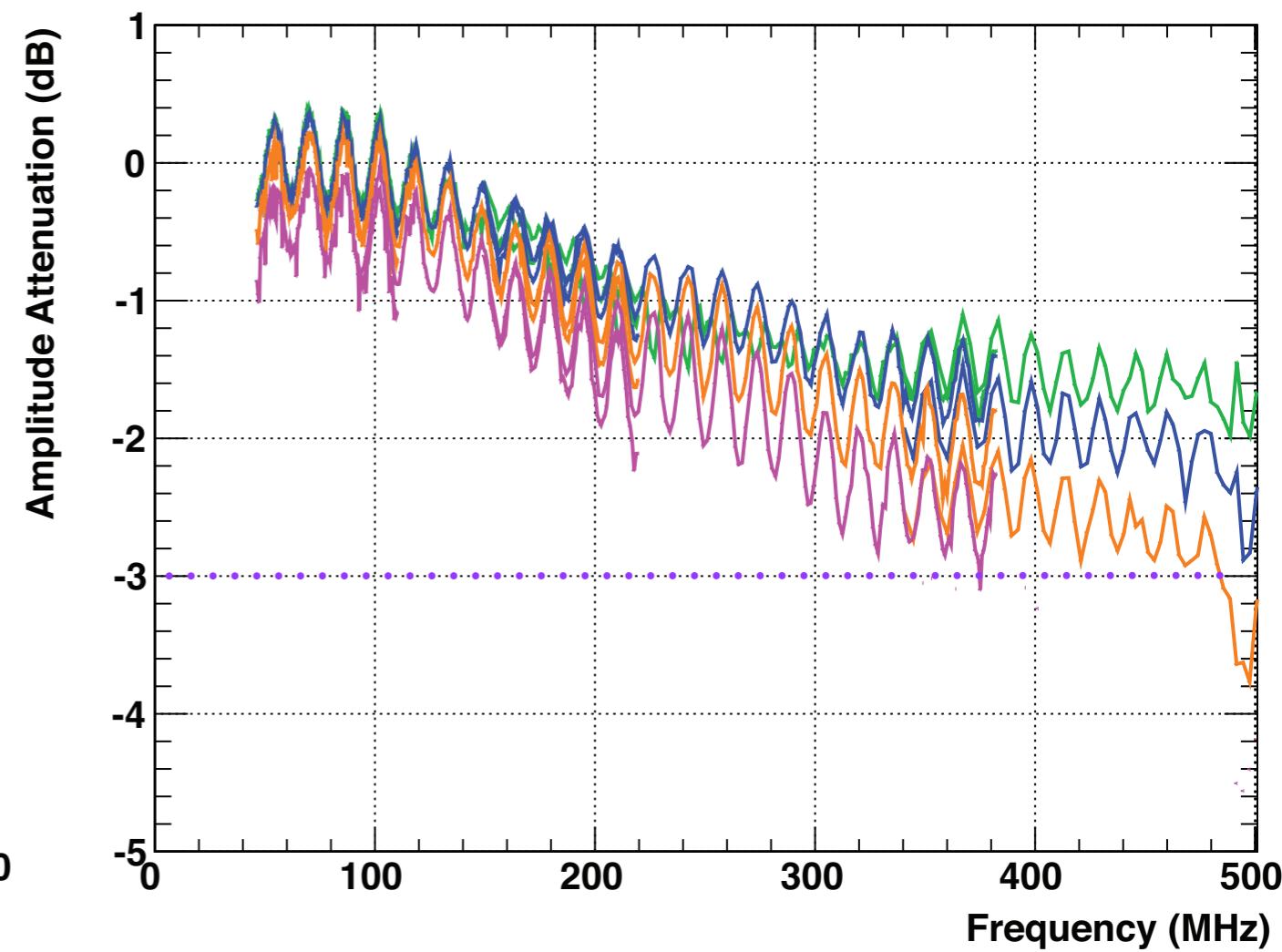
# Cross Talk and Band Width



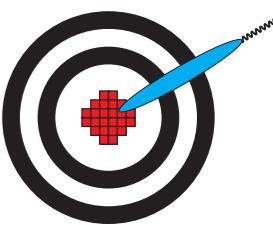
- ❖ Cross talk is less than 1% up to ~380 MHz
- ❖ Band width up to 480 MHz
  - ✿ Root cause of oscillating behavior under investigation



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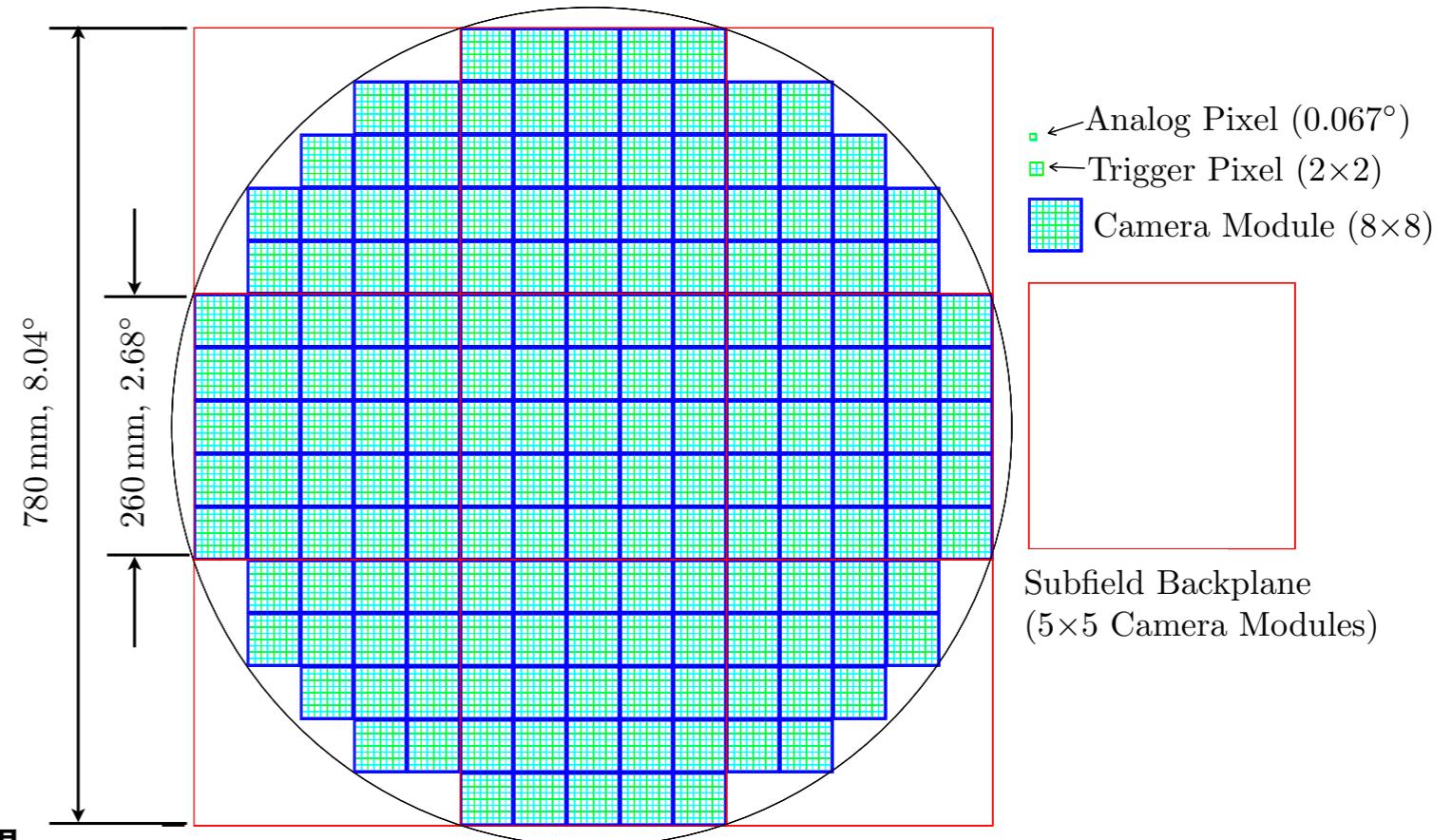
# SC-MST Camera Design

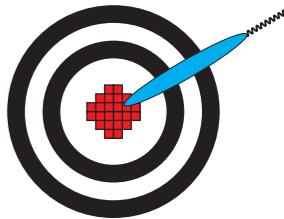


## ❖ SC-MST camera parameters

FOV	<b>8.0°</b>
Angular pixel size	<b>0.067°</b>
# of pixels per camera	<b>11,328</b>
Power consumption per camera (FE)	<b>800 W</b>
Weight per camera (FE+MAPMT)	<b>61 kg</b>
Total cost (FE+BE) for 50 CAMs*	<b>\$11M</b>

\*Assuming \$20/ch, which does not explicitly include labor for mechanical module assembly and calibrations





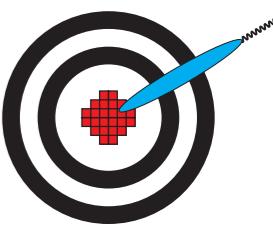
## ❖ SC-MST General requirements

- ✿ **Target cost: \$15 per channel**
  - ◆ Large # of pixels ~ 500k
    - More telescope, wider FOV, smaller pixels
  - ◆ Current cost estimates (conservative estimate)
    - Camera FE module: \$19/ch (11k channels), \$12/ch (500k ch)
    - Back-end electronics: \$6/ch (11k channels), \$4/ch (500k ch)
    - PMT, mechanical structure and calibrations not included
- ✿ **Reliability: low failure rate to minimize maintenance efforts**
  - ◆ Integration of “**necessary**” functionalities (small # of components)

## ❖ SC-MST requirements for camera front-end electronics

- ✿ **Waveform sampling at ~ 1 GSa/s**
- ✿ **Signal bandwidth > 380 MHz**
- ✿ **Cross-talk < 1%**
- ✿ **Look-back time: > 12  $\mu$ s**
- ✿ **Dynamic range: > 9 bits**
- ✿ **Readout (dead) time: < 30  $\mu$ s**
- ✿ **Trigger timing: < 4 ns**
- ✿ **Trigger segment:  $0.1^\circ \times 0.1^\circ \sim 0.2^\circ \times 0.2^\circ$**

# TARGET2 Architecture



❖ TARGET ASIC designed for CTA by G. Varner (Univ. of Hawaii)

